Tech Focus: Serial FPDP Board Roundup

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The Journal of Military Electronics & Computing

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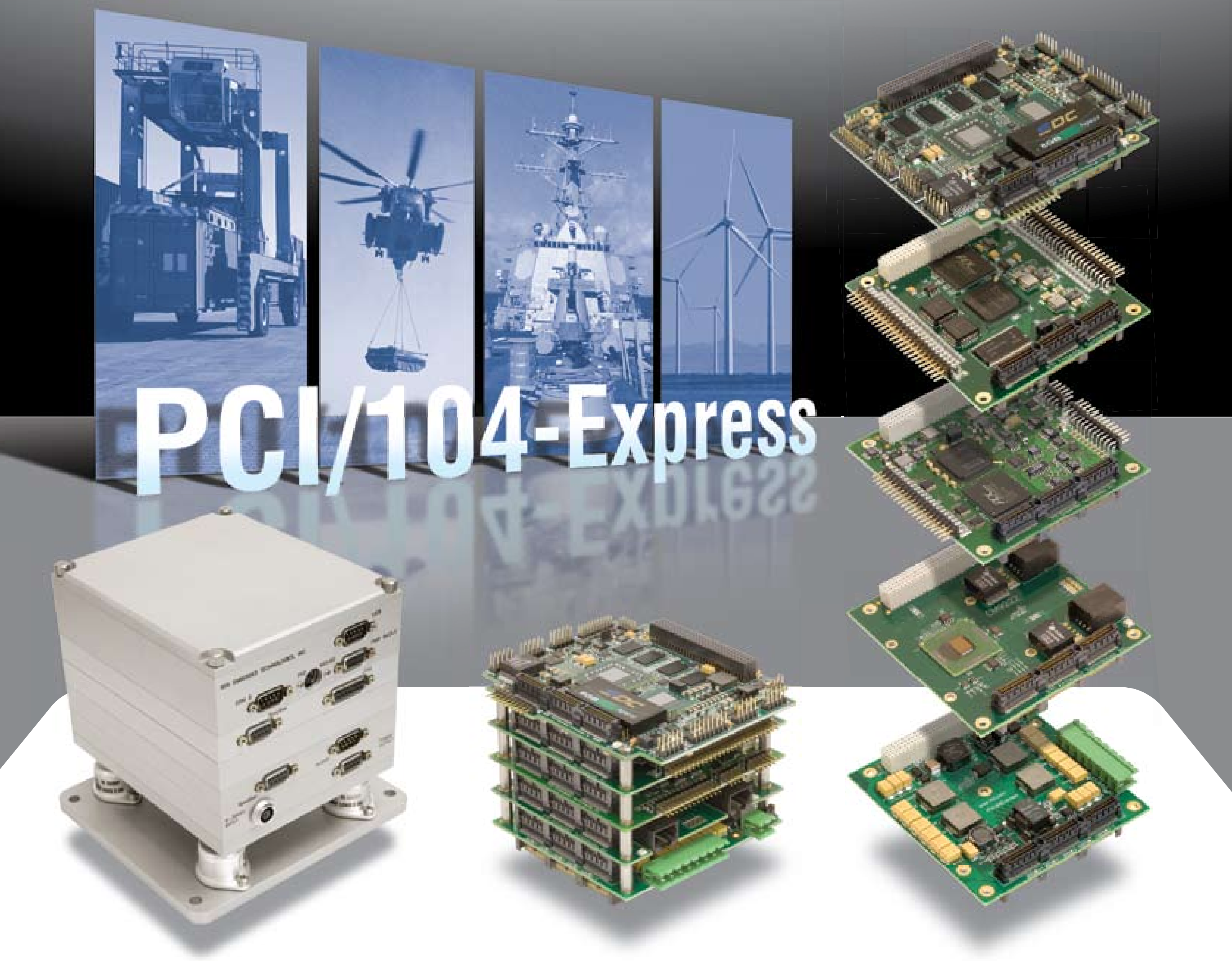

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Features

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Technology Focus

Serial FPDP Boards

COTS (kots), *n.* **1.** Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. **2.** Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

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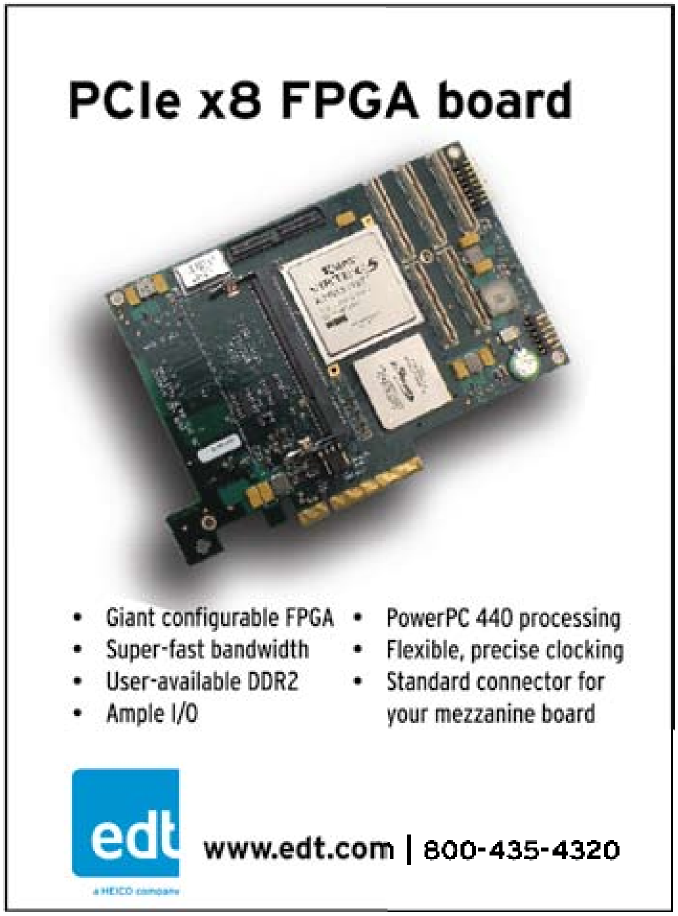
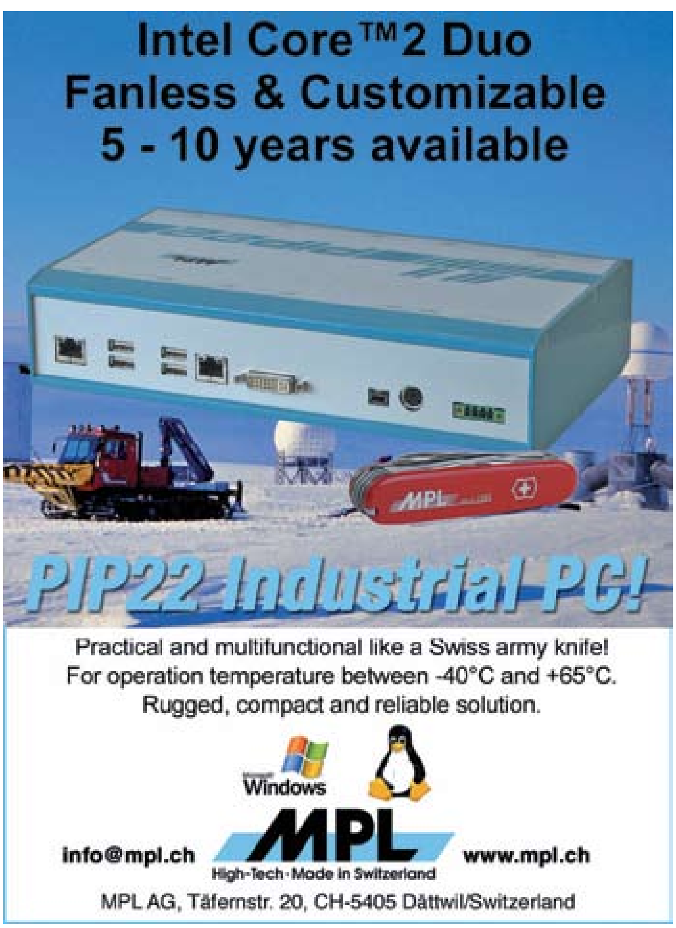
Secure Network Communications is among the most compute-intensive of today's military applications. Shown here, a Warfighter Information Network-Tactical (WIN-T) Increment Two test vehicle awaits movement instruction. The WIN-T Increment 2 embeds communications gear in the Commander's vehicles, enabling SIPR (Secure Internet Protocol Router) on the WIN-T platform.

(U.S. Army Photo)





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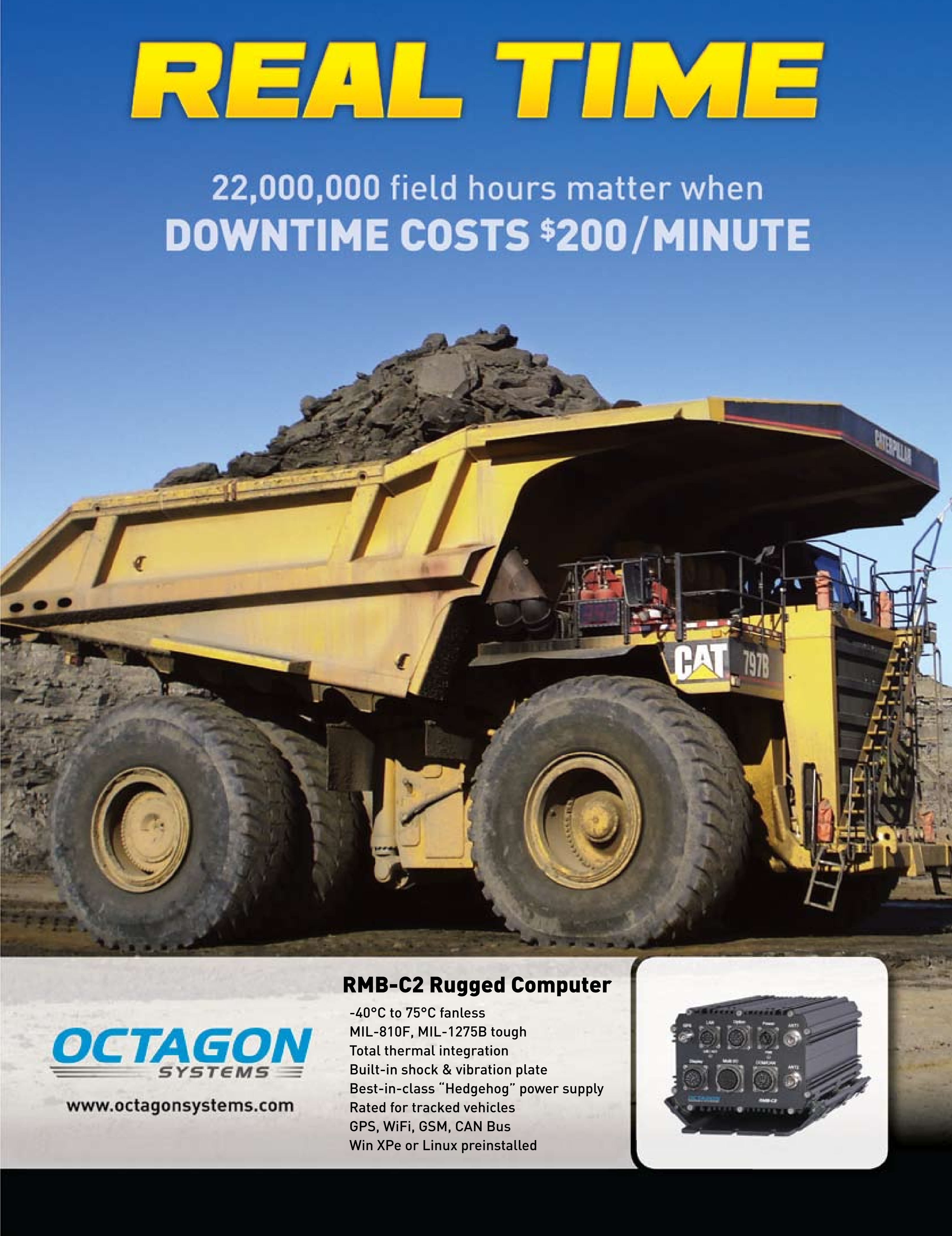
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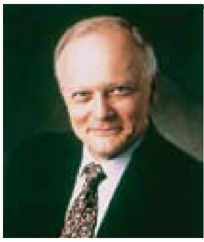

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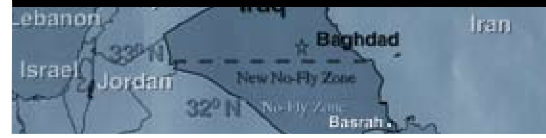

I Refuse to Fly Naked

Here we are starting another year. I'm a little late in writing this column, so I come to you armed with the knowledge that we have another nut trying to blow himself up in an airplane. Some time back someone sent me a cartoon showing a line of naked old people going through the boarding gate to get on an airplane and the comment was: "This security thing is going too far."

Life does not come without risk, although litigation in the courts seems to be focused on "zero risk or you must pay." People get injured and die, it's part of life. Of course, that's easy to say as long as it isn't you or someone close to you; but it is a fact and in general we need to accept that. We do need protection from people or entities that knowingly subject us to situations of risk without full and complete disclosure up front so we can determine our participation. This zero risk mentality is of high priority to lawyers, social extremists and politicians—well, sometimes politicians....when it creates good PR.

It's time we did a total re-think about how we fly and manage getting onto and off of aircraft. What we've been doing all along is updating a system that has been in place since we started flying passengers. I'm not saying I have any ideas, nor am I saying that any potential concepts will be low cost. But the current approach of continuing to whittle away at the individual passenger environment just isn't going to work. We need to have some out-of-the-box thinking on air travel and not focus on current preconceived approaches.

This now brings us around to the overall preparedness and tactics for dealing with terrorism. I don't find comfort in the Secretary of the Department of Homeland Security stating that this latest incident was an indication that "the system worked." And then she followed up the next day stating that what she was referring to was the interdepartmental communication following the incident and the departments' responses. As a government and as a people, we don't have a long interest level in anything. Maybe this latest incident will re-invigorate the concept that we are and have been under attack.

As a people, we Americans are optimists and have an enduring energy to find solutions and work through things. This latest incident should help us to accept that the mission isn't complete. The federal government's primary mission is the security of its populous. Once Congress gets back from its recess, let's hope that, unlike following 9/11, it focuses on moving forward rather than trying to start a witch-hunt on who "outside" of Congress is at fault. If the government organizes some form of brain trust with respect to air travel, it would be hoped that something significant would result. Most likely any proposal will include a significant amount of electronics providing opportunities for our community.

Last year was a year of turmoil for companies as well as individuals; although there is no clear vision that 2010 will be significantly better, we all think we see a light at the end of the tunnel. All indications are that the embedded military electronics market will continue to see growth not only in 2010 but also in following years. Statements like this are of little comfort to individuals whose employer has a minimal market share in the military programs and those who have a majority of their market share in a tenuous commercial market segment. This potential situation should not only be of concern to employees but also to PEOs and the military in general. Companies can fail because of their non-military market segment, and everyone needs to take a much broader view when reviewing potential suppliers.

Reading to this point, you may get the impression that all is doom and gloom. To the contrary, I see prosperity and opportunity for our embedded military market. This last year has been an exciting year for *COTS Journal*. Our readership is shifting due to a greater need for people up the decision-making process to understand the technologies that they are considering. We're also experiencing readership need for information on injecting more current commercial technologies into military applications. These are all indications of not only our growth, but also growth of our market. *COTS Journal* will continue to change with market needs and focus on providing what our readers require in order to facilitate their success in the development of products for the military. It's been our privilege and pleasure to serve you our readers and our market for over ten years, and we strive to exceed your expectations in this, our next decade of service. Our team wishes you all a happy, healthy and prosperous New Year. ▮▮

Pete Yeatman, Publisher
COTS Journal

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The Inside Track

Parvus Supplies Payload Interface Computers for MQ-5B Hunter UAV

Parvus' DuraCOR 810 mission computers have been integrated into Northrop Grumman's MQ-5B Hunter Unmanned Aircraft System (UAS). More than 40 DuraCOR 810 subsystems have been delivered to subcontractor Melhcorp and configured to operate as the Payload Interface Unit (PIU) for the Hunter UAV. These DuraCOR 810 units monitor, control and communicate between payloads on board the Hunter, as well as control the mounted payloads that include electronics and sensors.

Currently being deployed by the U.S. Army, the MQ-5B Hunter UAS (Figure 1) conducts battlefield surveillance using its multimission optronic payload. Flying over the battlefield, it gathers reconnaissance, surveillance, target acquisition and battle damage information in real time. The Hunter then relays this information via video link to commanders and soldiers on the ground. Melhcorp chose the Parvus DuraCOR 810 for the Hunter program because of its rugged modularity and MIL-STD-810F environmental compliance for extreme temperatures, shock/vibration and ingress. This tactical computer server integrates a low-power Intel Pentium M CPU together with a MIL-STD-704/1275 power supply in a rugged aluminum chassis with MIL-DTL-38999 connectors. Up to six spare PC/104(+) slots are available for integrators or Parvus to integrate mission-specific I/O functionality.

Figure 1

The MQ-5B Hunter UAV conducts battlefield surveillance using its multimission optronic payload. Flying over the battlefield, it gathers reconnaissance, surveillance, target acquisition and battle damage information in real time.

Parvus
Salt Lake City, UT.
(801) 483-1533.
[www.parvus.com].

Z-Microsystems Gets $2 Million Order from Airborne Surveillance Program

Z Microsystems has received a $2 million order for rugged, high-performance workstations and data storage for a forward deployed airborne surveillance program used for tactical intelligence missions. The program involves the collection of data by sensor-equipped aircraft. Workstations and data storage equipment supplied by Z Microsystems will support tactical intelligence collection, which includes facilitating accurate weapon targeting and identifying improvised explosive devices.

The military program is implementing Z Microsystems' ZXL2 workstations and TranzPak 7 data storage devices. The ZXL2 workstation is a low-profile, rack-mountable system with high-performance computing and graphics processing capabilities. The compact system is 3.45 inches (2U) high by 20 inches deep and supports up to three rugged hot-pluggable, removable drives, a slimline DVD-RW and a slimline floppy drive. User-friendly features include a front accessible power switch, two front accessible USB ports for rapid connectivity, and a quick-release top access cover for ease of service and hardware installation.

Z Microsystems
San Diego, CA.
(858) 831-7000.
[www.zmicro.com].

First Prophet Enhanced EW System Rolls off Production Line

Part of the Army's initiative to rapidly field signals intelligence capabilities that address the challenge of intelligence, reconnaissance and surveillance (ISR) recently rolled off the production line in Scottsdale. A team led by General Dynamics C4 Systems delivered the first Prophet Enhanced tactical signals intelligence system before a group of military customers including Brig. Gen. Thomas Cole, program executive officer for Intelligence, Electronic Warfare and Sensors for the U.S. Army.

Figure 2

The first Prophet Enhanced system, integrated into a Panther rapid-deployment command-and-control vehicle, will next undergo system testing and evaluation in Scottsdale.

The Prophet Enhanced system will enable tactical commanders to better "see," "hear" and "respond" to ISR information throughout the networked battlespace. The first system, integrated into a Panther rapid-deployment command-and-control vehicle (Figure 2), will next undergo system testing and evaluation in Scottsdale. The Army awarded the Prophet Enhanced contract to a team led by General Dynamics in February 2009. Built by BAE Systems, the Panther vehicle is a highly survivable, air-transportable

tactical vehicle that incorporates mine and ballistic protection for military personnel.

General Dynamics C4 Systems
Scottsdale, AZ.
(480) 441-3033.
[www.gdc4s.com].

Wind River Selected for NASA Ares Next-Generation Launch Vehicles

NASA has selected Wind River VxWorks 653 as the real-time operating system for the flight and command computers in the Ares I and Ares V (Figure 3) next-generation launch vehicles. VxWorks 653 will be the cornerstone for the Instrument Unit Avionics (IUA), providing guidance, navigation and control capabilities for the upcoming Ares I manned launch vehicle and the Ares V cargo vehicle, which will send future astronauts and large-scale hardware into orbit.

The Ares I rocket, a crew launch vehicle in development for NASA's Constellation Program, is the essential core of a reliable, cost-effective space transportation system that will carry crewed missions to the moon and out into the solar system. Ares V is NASA's cargo launch vehicle and the "heavy lifter" of America's next-generation space fleet, serving as NASA's primary vessel for safe, reliable delivery of large-scale hardware into space.

Figure 3

Artist's representation of an Ares V during SRB separation.

Wind River
Alameda, CA.
(510) 748-4100.
[www.windriver.com].

Military Market Watch

VME Holds Strong Position in a Wide Array of Mil/Aero Apps

The VME architecture is not only the embedded computing architecture of choice in the embedded military/aerospace COTS market, it has also proven to be an extremely versatile architecture in the COTS market. According to the most recent research into the embedded mil/aero COTS market conducted by VDC Research Group in December 2009, VME is deployed in a widely varying array of mil/aero applications.

The data shows (Figure 4) that integrated system-level VME COTS systems sold by merchant VME vendors in North America went into a diverse set of end applications led by radar and command and control applications. Radar (30%) and command and control (28%) applications consume nearly 60% of all merchant VME shipments to North America. These two application areas have traditionally been two of the largest consumers of COTS boards and systems in the military/aerospace, so it is unsurprising to find that they lead the VME COTS market as well.

However, the other 42% of the North American VME systems market is consumed by a lot of different applications. VME has proven itself to be a very versatile architecture and provides unparalleled ruggedization, so it has found a home in virtually all embedded mil/aero end applications. In many mil/aero applications it is more a matter of finding a reason not to use VME rather than a reason why the architecture is a fit.

With the addition of the VPX architecture to the VME family, it is expected that VME's versatility and adaptability will only increase over time. VPX products providing high bandwidth and the availability of smaller 3U form factor products will allow VME to fit into even more applications, particularly new high-performance mil/aero applications. It is likely that the application distribution of VME will become even more diverse and less concentrated around radar and command and control in the future as a result of VPX, which will allow VME into new application types.

The widely varying number of applications consuming VME systems shown here is similar for VME board-level products. It can be expected that that VME and VPX will continue to be deployed in virtually every COTS application classification into the foreseeable future. For more information please contact Eric Heikkila of VDC at: erich@vdcresearch.com.

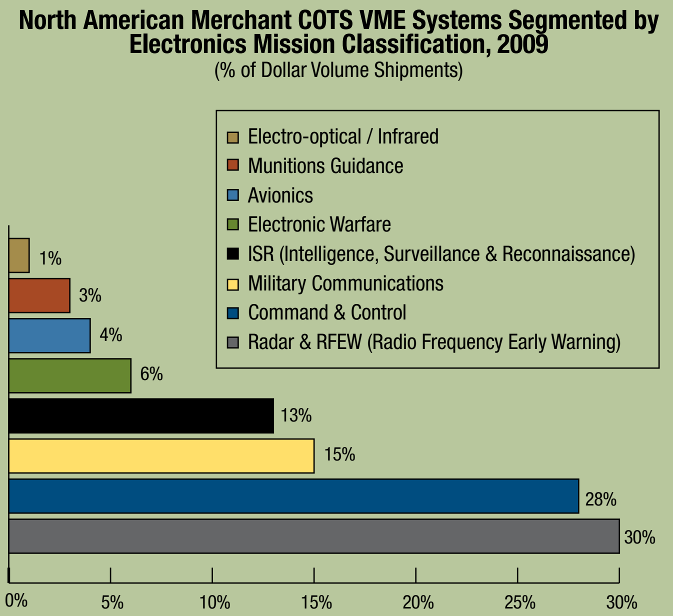

Figure 4

Integrated system-level VME COTS systems sold by merchant VME vendors in North America were used in a diverse set of end applications, with radar and command and control applications leading the pack.

VDC Research Group
Natick, MA.
(508) 653-9000.
[www.vdcresearch.com].

BAE Systems Equips U.S. Army Helicopters with Infrared Countermeasures

BAE Systems has successfully installed the Advanced Threat Infrared Countermeasures (ATIRCM) system on U.S. Army CH-47D Chinook aircraft. The ATIRCM system (Figure 5) is a laser-based, directable countermeasures system that protects helicopters against attack by missiles.

The ATIRCM system, including the AAR-57 Common Missile Warning System, greatly enhances overall aircraft survivability against current and evolving threats. Its installation follows a series of rigorous qualification, field and flight tests. The first systems were installed ahead of the December 15 deadline for the Army's ATIRCM quick-reaction capability program.

Figure 5

A U.S. Army helicopter flies over the BAE Systems Test Range for Advanced Threat Infrared Countermeasures (ATIRCM).

BAE Systems
Nashua, NH
(603) 885-4321.
[www.baesystems.com].

Event Calendar

February 2
AFCEA West 2010
San Diego, CA
www.afcea.org

February 9
Real-Time & Embedded Computing Conference
Huntsville, AL
www.rtecc.com

February 11
Real-Time & Embedded Computing Conference
Robins AFB, GA
www.rtecc.com

February 24-26
AUSA Winter
Ft. Lauderdale, FL
www.ausa.org

March 9
Real-Time & Embedded Computing Conference
Chicago, IL
www.rtecc.com

March 11
Real-Time & Embedded Computing Conference
Minneapolis, MN
www.rtecc.com

April 13
Real-Time & Embedded Computing Conference
Melbourne, FL
www.rtecc.com

April 15
Real-Time & Embedded Computing Conference
Eglin AFB, FL
www.rtecc.com

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sallyb@rtcgroup.com

Target Report

Five Compute-Intensive Defense Application Areas

New Solutions Attack the Defense Industry's Most Compute-Centric Problems

As increasing amounts of military system functionality become computer-based, the embedded industry continues to craft more advanced solutions and architectures to suit current and next-gen defense needs.

Jeff Child
Editor-in-Chief

There's a trend that should be obvious, but is often overlooked at higher echelons of the defense industry: More and more of system functionality is now implemented as software running on single board computers, replacing legacy systems based on hard-wired electronic assemblies. The drive for ever more compute density has become the mantra for many of today's advanced military programs. In this, our first Target Report of the year, we analyze five compute-intensive military applications and explore how today's crop of embedded computer form factors and technologies is serving their needs.

As we researched the various programs, it became obvious that there are, of course, many more than five compute-intensive military applications to choose from—there are so many that fit that definition. Ultimately, it was boiled down to the following five somewhat general categories:

- Multi-Sensor Image Processing and Exploitation
- Aircraft-based Cluster Computing
- Persistent Surveillance on UAVs
- Secure Network Communications
- C4ISR

The vast amount of sensor data streaming into ISR sensors are demanding ever more processing to exploit the data and make it useful for warfighters. The sidebar "Multi-Sensor Image Exploitation Using Smart Processing" in this article explores that topic.

Some military reconnaissance aircraft have up to seventy computer systems dedicated to different aspects of the surveillance mission. The bylined sidebar "Cluster Computing Suits Up for Aircraft Duty" by Trenton Systems on p.16 in this article, discusses the architectures suited to those needs. Persistent surveillance requires highly compute-intensive imaging capabilities as a UAV remains in an area to detect, locate, characterize, identify, track, target and re-target threats. The bylined sidebar "GPU-based Processing Solves Persistent Surveillance Challenges" by Mercury Computer Systems on p.18 in this article explores the issues invloved.

The combined pressures of high bandwidth, security and data processing make today's military comms systems among the most compute-hungry around. The problems and solutions are explored in the article "Secure Network Communications Pushes Compute Limits" by Kontron on p.22 of this section. And, last but not least, a variety of deployed high-performance systems can be classified as C4ISR (Command, Control, Compute, Communications, Intelligence, Surveillance, Reconnaissance). The article "Next-Gen Processor Technology Redefines Compute Density" by Extreme Engineering Solutions on p.30 of this section, talks about how C4ISR systems are typically very compute intensive with high communication bandwidth requirements. They are deployed in harsh environments, and they have Size, Weight, and Power (SWaP) constraints.

High Compute-Density Needs across the Industry

Beyond those five application areas, the defense industry if rife with programs that push the limits of computing needs. Many of these are driven by the general desire for autonomous operations, along with real-time, or closer to real-time decision making. Automatic Target Recognition, for example, is in some ways a fairly established technology. But systems that can acquire and track targets completely autonomously—doing so when the target and shooter are moving—call for a whole different level of computing. Signal Intelligence (SIGINT) is another area where

continued on page 20

Multi-Sensor Image Processing & Exploitation

Multi-Sensor Image Exploitation Using Smart Processing

New generations of ISR sensors are surveying ever wider areas with constantly increasing levels of sophistication. Electro-optic infrared (EO/IR), synthetic aperture radar (SAR), hyper-spectral imaging (HSI), laser radar (LADAR), SIGINT and COMINT systems scan vast spaces and collect an enormous amount of raw data. Mounted on long-endurance, unmanned platforms, an array of these sensor technologies can deliver the persistent surveillance necessary to find and fix an elusive, insurgent enemy.

Experience shows, however, that the volume of multi-sensor data collected in just one mission overwhelms the human imagination and crushes existing tasking, processing, exploitation and dissemination (TPED) architectures (Figure 1). How can we extract truly valuable information from all that data and get the information to the people who really need it, when they need it?

Today's image exploitation systems are already overloaded at two levels by the current volume of data. On the first level, deployed tactical data links cannot transmit the full data streams generated by multiple sensors. On the second level, the volume of data that is successfully transmitted to a ground station exceeds the current TPED architecture. An estimated 90 percent of the received data is not even examined—it essentially just "falls on the floor" and remains unused.

The situation requires a new approach, a novel TPED architecture that calls upon next-generation computing technology to multiply the effectiveness of human analysts and reduce the delivery time for actionable intelligence. This "Smart Processing" architecture performs the initial stages of processing and exploitation directly on the tactical platforms, rather than on the ground stations. Both analysts and the remote devices of forward-deployed personnel direct the processing and exploitation in an on-demand fashion. Computing, communications and networking are located as close as possible to the critical tactical users.

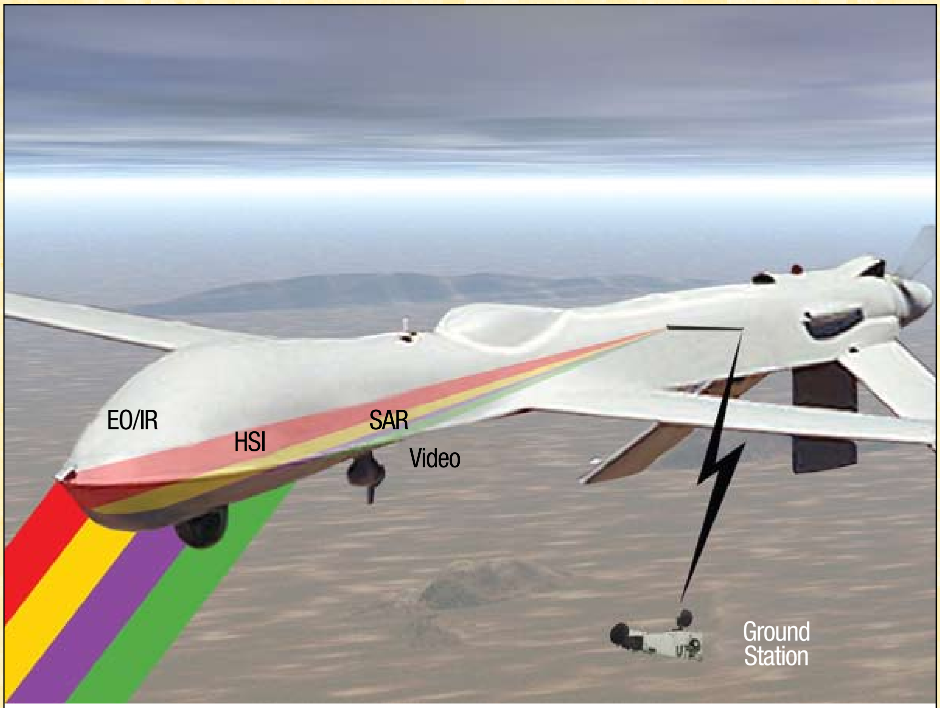

Figure 1

The huge volume of multi-sensor data collected in just one UAV mission overwhelms existing tasking, processing, exploitation and dissemination (TPED) architectures.

A Smart Processing architecture first directs the multi-sensor data streams to an on-platform real-time computing system. This embedded computer uses advanced signal and image processing algorithms to make a first pass through the incoming data, prioritizing the data for downstream analysis, and tasking the collection of additional data to more rapidly find and fix targets. For example, an aided target recognition (AiTR) algorithm can examine large numbers of SAR images and/or motion imagery and provide an alert to potential threats.

Smart Processing also includes real-time cross-cueing, using multi-intelligence sensors to detect, track and engage threats with a higher degree of precision, supporting multiple simultaneous users and delivering mission-specific, tailored sensing to warfighters on the tactical edge. These are just a few examples of Smart Processing's potential capabilities.

Unleashing these capabilities demands a huge leap in deployed processing power, based on embedded, real-time computers that are small, powerful and rugged. Those are just the baseline requirements. Successful deployments also require that these computer systems be inherently networkable, and able to be configured and re-configured dynamically into flexible, mission-focused networks.

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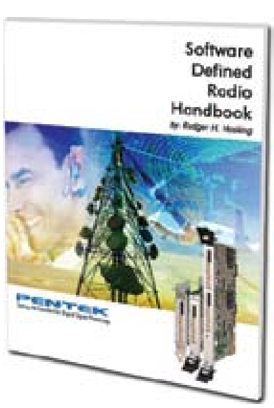

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Cluster Computing Suits Up for Aircraft Duty

Jim Renehan, Director of Marketing, Trenton Systems, Inc.

Surveillance aircraft may represents just a small slice of the overall military defense market, but they exemplify many of the challenges facing the rackmount system designer. Surveillance aircraft provide location information and near-real-time situational analysis—a critical role in today's military, where information is as essential as firepower. Fulfilling this mission requires an enormous amount of computational horsepower.

A typical airplane may have seventy computer systems dedicated to different aspects of the surveillance mission. The computer systems must also be flexible enough to handle the multiple system configurations used in the aircraft. The computers must have a long service life and a stable system configuration to meet the aircraft's long deployment and refurbishment schedules.

Weight and space are at a premium on a surveillance aircraft. Additional computer hardware has an exponential effect on the cost of operating the aircraft. In addition to increasing the fuel costs, extra equipment weight creates mission delays due to the need for more frequent mid-air refueling. Trenton addressed both the space and weight issues by developing a shallow-depth chassis made out of lightweight aluminum. Figure 1 shows an expanded view of a typical Trenton Systems platform designed for use in a surveillance aircraft application.

Figure 1

By taking advantage of cluster computing, this lightweight chassis can replace up to sixteen conventional 1U chassis.

The most common rackmount chassis used on the aircraft has a depth of 18 inches (45.72 cm) and a 5U chassis height. Each system has a multi-segment PICMG 1.3 backplane that enables multiple SBCs or system host boards (SHBs) to function in a single chassis. Other chassis design elements include individual SBC segment power control, quick access storage drives, corrosion-resistant metal work, a high-performance cooling system and armored cable sleeves for vibration protection.

The backplane is often a frequently overlooked component of an embedded computing system, but it is an essential element of a high-performance embedded design. Today's higher bandwidth card-to-card interfaces such as a PCI Express (PCIe) demand robust backplane designs in order to maintain optimum system throughput. For this system, Trenton engineers used its four-segment BP4FS6890 backplane. This multi-segment PICMG 1.3 backplane is available in server-class or graphics-class configurations. The PICMG 1.3 backplane supports one or more SHBs, as well as industry standard COTS option cards for functions including communications, video, sound and data storage. This design allows designers to mix and match single board computer capabilities based on the needs of the application. Two types of Trenton SHBs are used in surveillance aircraft: the Trenton TQ9 System Host Board and the Trenton MCXT System Host Board. Each SHB features quad-core processors with Intel Virtualization Technology (Intel VT).

Persistent Surveillance on UAVs

GPU-based Processing Solves Persistent Surveillance Challenges

Anne E. Mascarin, Product Marketing Manager, Mercury Computer Systems

Persistent surveillance requires highly compute-intensive imaging capabilities because the aerial vehicle must remain (on demand) in an area to detect, locate, characterize, identify, track, target and re-target threats. These imaging tasks must be performed and processed in real time, on multiple sensor data streams, so that actionable information is available to the warfighter.

Producing high-quality imagery on a mobile platform like a UAV poses some interesting challenges, including the motion of the platform and the resulting image perspectives. Onboard exploitation techniques and algorithms are employed to remove the resulting distortion present in the original imagery. Ortho-rectification uses geometric projections to remove the distortion present in the original imagery to produce geometrically correct images.

Geo-registration (the process of adjusting an image based on the relative similarity between the raw sensor data and a reference image) can be performed to stabilize the image, along with geo-location (the process of comparing the geo-registered image data to known geographical coordinates) to yield the most accurate image. Finally, this processed data, which still represents individual sensor streams, must be "stitched" or "mosaic-ed" together to create a fused image. Together, the real-time processing requirement, intense algorithmic computation, and parallel processing aspect of onboard exploitation present a huge computational load.

The long mission duration aspect of persistent surveillance (frequently multiple days) demands minimal power consumption. Often, imaging subsystems are the last to be added onto the airframe, and are subsequently allotted the smallest portion of the power budget.

Clearly, imaging subsystems based on processors that feature the lowest power consumption and the highest performance (the GigaFLOPS/watt metric) are the best choice for persistent surveillance applications. Many CPU-based boards don't meet these stringent GFLOPS/watt requirements. Graphical Processing Units (GPUs), first introduced by NVIDIA in 1999, have always had very high GFLOPS/watt metrics. Given their parallel performance potential and low power consumption, why haven't GPUs been utilized much for compute-intensive embedded computing? Programmability is one reason, and upgradeability is another.

Figure 1

The Sensor Stream Computing Platform is a GPU-based development platform that enables users to design, simulate and implement data exploitation algorithms in a 6U VXS form factor.

The software environment for GPUs has been notoriously non-intuitive even to proficient embedded programmers. The environment is based on graphics primitives—not high-level language constructs or even CPU assembly variants. And the basic structure of programming tools for GPUs has not offered the optimizations that programming languages for CPUs do. GPGPUs (General Purpose GPUs, from ATI, NVIDIA and others) offer familiar constructs such as well-defined APIs and indexed matrix operations.

Historically, GPUs have not been easily upgradeable; they have been discrete components soldered directly onto the printed circuit boards. Upgrading the chip as new versions become available would require a complete board respin. Many of today's GPGPUs, however, are available in a mobile PCI Express module (MXM); an easy to insert format that supports easy upgrades when new, faster GPGPUs are available. An example system that employs GPU-based processing is Mercury's Sensor Stream Computing Platform (Figure 1), a GPU-based development platform for embedded, sensor stream computing and exploitation. It is an environment that enables users to design, simulate and implement data exploitation algorithms in a low-power, high-performance 6U VXS form factor.

SIDEBAR

Intel Architecture Invades Embedded DSP Arena

Ian Stalker, DSP Product Manager
Curtiss-Wright Controls Embedded Computing

Floating point processors are an essential component of military digital signal processing (DSP) systems. For approximately the last ten years, the evolving series of Power Architecture (formerly "PowerPC") processors with AltiVec have earned the lion's share of the aerospace and defense signal processing market. Recent advances in Intel microprocessors though, for the first time, now provide an attractive alternative to AltiVec in the COTS military signal processing arena.

Theoretically, demanding military DSP applications such as radar, sonar and signal intelligence can be accomplished with either fixed-point or floating-point numerical representation. A key reason that floating point arithmetic is preferred is that it reduces software development costs. DSP algorithms rely heavily on multiplication, and to a lesser extent, division operations. Intermediate results during calculation can result in over-flow and under-flow conditions using fixed point. There are techniques to manage these undesired circumstances, but they require the use of complicated software that is slower to develop and slower to run.

A recent survey of signal processing customers conducted by Curtiss-Wright Controls spotlighted the need for floating-point performance. Ninety-four percent of the surveyed respondents stated that they used the AltiVec floating-point unit. Survey respondents also said that memory performance, and closely related, inter-processor bandwidth, are considered more important than a signal processing board's raw FLOPs rating. These responses indicate that many users are doing signal processing on streaming dataflows, which are sensitive to the computer's memory performance.

Survey respondents said memory performance and inter-processor bandwidth are more important than a signal processing board's raw FLOPs rating.

The next decade promises new developments in DSP processing. One factor will be the fate of AltiVec. The latest high-performance Freescale processor, the eight-core QorIQ P4080, while an excellent CPU for single board computer designs, with integrated memory controllers and both PCIe and SRIO interfaces, does not have an AltiVec unit. Instead, the P4080 features the standard Floating Point Unit (FPU), which is not the vector processor type required to attain the floating-point performance required for signal processing applications.

Meanwhile, the demand for media processing in personal computing continues unabated. To address this demand, Intel has developed a vector processing technology generically known as SSE (Streaming SIMD Extensions). Like AltiVec, SSE is a 128-bit wide processing unit, capable of simultaneously operating on four single-precision (32-bit) floating-point values. SSE also features support for double-precision (64-bit) floating point, a feature that was not available in AltiVec. Since its introduction, Intel has continued to add new SSE features and instructions, culminating in the current implementation in Core i7 processors, SSE 4.2. Using SSE, the Core i7 can issue simultaneous add and multiply instructions, resulting in a peak rate of 8 floating-point operations (FLOP) per clock cycle. Each Core i7 processor has its own SSE unit, so the raw floating-point performance scales with the number of cores.

It is difficult though to make a simple comparison of raw GFLOPs and kernel benchmarks between Intel and Freescale processors. Real-world DSP application performance is a complex interaction of instruction mix, cache size and latency, SDRAM performance and the utilization of shared resources. But on a clock for clock basis, SSE performs similarly to AltiVec on key signal processing benchmarks such as a 1K complex FFT. Along with SSE, the new generation of Intel Core i7 processors also offers significantly improved memory performance and overall cache performance compared to the prior generation Core 2 Duo architecture. The Core i7's improved cache performance stems from its three-level on-die cache. As vector sizes, (including twiddle factors for FFTs) extend past the size of the L1 cache, the L2, L3 cache and SDRAM performance quickly dominate the throughput of the processor.

added computing muscle serves an endless appetite for security-critical data sifting.

In general, military UAVs and their payloads are by definition compute intensive, and will only become more so. Tasked to capture and download secure, encrypted surveillance data, today's advanced surveillance UAVs require a lot of communications overhead. At present, U.S. military recon UAVs relay almost all UAV captured data to the ground to process it for interpretation and decision making. The goal is to make use of onboard processing muscle to enable UAVs to instead relay the results of their data processing to the ground for decision making.

The benefit is reduced reliance on data link rates in certain applications, particularly imagery collection. In today's UAVs, image formation is done in the air and then sent down. For payloads of the future, the trend is toward fusing data and sending down just the things that are different than the established data base—or some other way of compressing and fusing the information. All of this helps overcome the defining constraint for these systems: the limitations of data link bandwidth.

Waveform-Driven Applications

Meanwhile, waveform-intensive applications like radar and SIGINT seem to have no end to their appetite for signal processing power. Faster DSPs coupled with a broader range of IP cores and development tools for FPGAs are joining forces to form new DSP system architectures. Using those building blocks, board-level subsystems must quickly acquire and process massive amounts of data in real time. As FPGAs evolve to ever greater sophistication, complete systems can now be integrated into one or more FPGAs. That in turn means that the rack and backplane-based systems based on FPGAs offer the compute muscle of yesterday's supercomputers. Modern radar systems are operating over an ever increasing frequency range. Analog conversion technology—both A/D and D/A converters—are also feeding the radar needs of the military.

System developers can now build radar receiver systems with a higher instantaneous bandwidth thanks to the converters, and can handle the corresponding increase in compute power required to process the received data streams using FPGAs. The ASIC-based radar design approaches of the past can achieve the performance needed, but that path lacks the flexibility inherent in designs based on FPGA technology. A wealth of FPGA board-level products are available aimed specifically at this area.

Disruptive Technology: GPGPUs

While the attraction of FPGAs in high-end military systems is today as solid as ever, a disruptive technology could have the potential to unseat them. This disruptive technology is the emerging idea of using the latest crop of high-performance graphics processors to handle general-purpose processing tasks. Driven by architectural advancements in recent years, the scope of applications to which GPUs can be applied has grown dramatically. Feeding this notion of GPUs as general-purpose processing engines, NVIDIA developed a parallel computing architecture called CUDA (an acronym for Compute Unified Device Architecture) that addresses a key weakness of FPGA parallel processing systems: the complexity of programming them. CUDA is the computing engine in NVIDIA graphics processing units (GPUs) that is accessible to software developers through industry standard programming languages.

GPGPU technology can, for example, deliver more capable detection systems, increase the autonomy of unmanned vehicles and provide a wide-ranging improvement in survivability across a broad spread of applications. According to GE Fanuc, a major defense prime contractor has a radar application to the CUDA environment and achieved a 15x improvement in performance. In another case, according to GE Fanuc, the productivity of the CUDA environment is illustrated by the brief time—just over two weeks—it took another prime contractor to migrate an application to the CUDA environment.

This focus of computer-centric military applications seems to be in synch with the direction upcoming DoD budgets will shift to. Even as the political landscape changes, and forces within the government drive the budget down, the embedded computer component of the overall DoD budget is going to increase dramatically—a trend that's been occurring consistently now for several years. ▮

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Secure Network Communications Pushes Compute Limits

The multiple pressures of high bandwidth, security and data processing make today's military comms systems among the most compute-hungry defense applications.

Christine Van De Graaf, Product Manager and
David Pursley, Field Applications Engineer, Kontron

New and evolving technology initiatives such as Brigade Combat Team Modernization, JTRS (Joint Tactical Radio System) and WIN-T (Warfighter Information Network-Tactical) rely heavily on secure communications and sharing vital information on the battlefield, linking ground command centers to individual soldiers mobilized via land, sea and air. Representing an incredibly diverse set of application requirements, these complex systems frequently require greater communication bandwidth, broader functionality and smaller footprints-at the same time accounting for the military's supreme need for security, mobility, flexibility and ruggedness.

Military design is deeply entrenched in VME and CompactPCI platforms, but is also evolving significantly based on the need for increased bandwidth and faster, more sophisticated signal processing. Designers are not abandoning these tried and true platforms, but are embracing new and compatible architectures offering new standards of performance built solidly around the military's keen eye on using technology to its fullest potential. For example, significant portions of the WIN-T program are using the MicroTCA architecture, offering ideal native support of Internet-protocol-based network topologies found in the network-centric nature of WIN-T. Platforms such as Computer-on-Modules (COMs) are going further in extreme military design, offering rugged and extended temperature options in tandem with small mobile and power-efficient design tenets.

Figure 1

Data and voice communications for mobile military applications have very specific requirements. Devices must deliver high-bandwidth performance within demanding temperature ranges as well as high shock and vibration environments.

Figure 2

MicroTCA platforms have already been adopted by Lockheed and Boeing's P-8A program, and actively deployed by Harris and BAE in WIN-T applications.

VPX extends legacy VME beyond its own inherent signal processing capabilities, adding high-frequency signal processing along with a reliable fabric solution that facilitates onboard checking and retransmission.

Advanced Secure Comms

WIN-T has a key role in defining and advancing secure network communications for military applications, being implemented in increments that bring greater levels of networking capabilities to various deployed units and ground commands. Increment 1, defined as "networking-at-the-halt," is a rapidly deployable system that provides roll-on/roll-off mobility; this in turn delivers Internet-based connectivity to the warfighter, satellite and line-of-sight connectivity, and DISN (Defense Information Systems Network) services down to the Battalion level. Increment 2 is defined as "networking-on-the-move"-the first step in developing a mobile infrastructure on the battlefield-and extends a communication network down to the Company level. On-the-move broadband networking capabilities use satellite and radio links, focusing on Brigade Combat teams and allowing them to operate on the move (Figure 1).

WIN-T Increment 3 Underway

Increment 3, which is at its earliest stages, provides full network mobility and introduces an air tier of connectivity. The result is a multilayered architecture that includes traditional line-of-sight, airborne through the use of Unmanned Aerial Vehicles (UAVs), other airborne platforms and satellites. Building on previous Increments, Increment 3 enables the full objective mobile, tactical network distribution of C4ISR (Command, Control, Communications and Computers, Intelligence, Surveillance and Reconnaissance) information via voice, data and real-time video. Soldiers have more robust connectivity and greater network access via military specification radios, higher bandwidth satellite communications (SATCOM) and line-of-sight (LOS) waveforms, an air tier (LOS airborne relay), and integrated Network Operations enabling video teleconferencing and other collaboration applications.

For embedded designers, creating this versatile mix of tailorable, networked organizations means developing or up-

Figure 3

The OM5080 MicroTCA system provides efficient cooling by a push-pull arrangement of dual fans, which are controlled by system management. In combination with the 2U form factor, it allows the use of powerful cooling at performance levels beyond the scope of front cooled 1U or 2U servers.

grading capabilities, and eliminating platforms whose size, weight and power constraints limit performance or battle-readiness. Designers are challenged to build in greater amounts of bandwidth, smaller form factors and proven ruggedness far beyond technologies found in earlier military initiatives.

ATCA and MicroTCA

ATCA and MicroTCA are gaining significant ground in high-performance military network computing due to their standards-based, rugged, high-bandwidth performance in a small footprint. In particular, the secure network approach to warfare is an ideal fit for the features of the ATCA and MicroTCA platforms, characterized by high processing capacity, extremely high communication bandwidth and high availability designed into a small form factor. MicroTCA is a good design platform for IP-based network applications, offering native support for IP-based network topologies packaged with high bandwidth, increased computing power and the small form factor frequently required by these network-centric applications (Figure 2).

For example, MicroTCA's high bandwidth for both communications and computing results from up to 12 compute blades on a single backplane, potentially all using a multicore processor. A 3U or 4U system could integrate as many as 24 cores designed into MicroTCA's very small footprint. MicroTCA designs can also tap as many as 21 high-speed serial connections on the backplane, with each connection delivering bandwidth of 2.5 Gbits/s. A broad range of communications bandwidth capacities is possible-ranging from 40 Gbits/s to greater than 1 Terabit/s-based on how each system is implemented. Figure 3 shows an example MicroTCA system.

COM Express for Space-Constrained Apps

Ruggedized COM Express modules bring the latest technology in the smallest size to COTS-based military networking applications. Unmanned vehicles, field devices such as Software Defined Radios used by individual soldiers, and embedded devices enabling secure communications systems are benefiting from the compute power and reliable performance being delivered by these compact components.

Based on the compact Intel Atom solution, COMs balance performance with the SwaP (Size, Weight and Power) issues critical to mobile networks and ideal for small mobile and extremely energy-efficient devices such as man-wearable systems. Designed today for use in extreme conditions, COMs offer industrial temperature ranges of -40° to +85°C as well as the necessary tolerances for high reliability in terms of shock and vibration resistance.

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VPX for Rugged Systems

VPX has a solid foothold as the future of rugged military systems, due to its ability to provide high-frequency processing as well as a reliable fabric solution that facilitates onboard checking and retransmission. VPX builds on the processing capabilities of VME, combining robustness and excellent EMC-fundamental strengths of the VMEbus architecture-with new high-bandwidth connector capabilities for high-speed differential signaling over the backplane, and offering support over wider operational temperature ranges with cooling methodologies. For example, 10 GbE takes in a fast data rate and dispatches it to several processors that manage the workload in parallel.

Designing in this kind of functionality highlights VPX as an ideal platform for network-centric military systems, leveraging more I/O per slot and higher computing density from available processors and chipsets. VPX packs these features in a smaller 3U form factor, well-suited to many of the new real-time, data-intensive and network-centric applications that require reliable performance in harsh environments.

Secure, networked communications are designed to both equip soldiers and ensure their safety throughout the base of military operations. Designers are answering this critical and compute-intensive challenge with a growing technology arsenal-effectively leveraging more I/O per slot, achieving higher computing density from current processors and chipsets, and delivering better power-to-performance ratios that bring safety and technology leadership to our modernized battlefield. ▮

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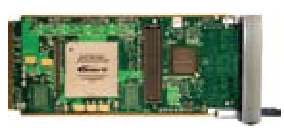

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Next-Gen Processor Technology Redefines Compute Density

The trend toward net-centric warfare and moving more data to the battlefield "edge"countinues. That's driving demand for highly integrated compute technologies such as the latest Intel Core i7 processor and 3U VPX.

Ben Klam, VP of Engineering, and
Dave Barker, Director of Marketing,
Extreme Engineering Solutions

The demands of today's advanced military applications require system architects to constantly push the design envelope. These demands are coming from multiple fronts. The military is facing new enemies, which necessitate new war fighting strategies. The military is also facing new threats, such as IEDs, which necessitate new defensive and offensive techniques to keep soldiers out of harm's way. Unmanned vehicles and machines are increasingly being used not only to perform dangerous missions but also for surveillance and reconnaissance.

There is a continuing trend toward network-centric warfare and moving more data to the "edge," that is, to the soldiers on the battlefield to give them more accurate real-time data. To meet the needs of these new demands, systems must be smaller, lighter and faster-more processing power and bandwidth while at the same time reducing total footprint. Two technologies that together are meeting these demands by redefining compute density are the Intel Core i7 processor and 3U VPX.

To address these new warfare demands, the trend has been to move more processing into the field using small deployed systems. Military applications span the range of the computing spectrum, but the type of applications these small, deployed high-performance systems satisfy can be classified as C4ISR (Command, Control, Compute, Communications, Intelligence, Surveillance, Reconnaissance). Even within C4ISR there is a wide range of applications, each having unique requirements. However, many deployed C4ISR applications share some common attributes. They are typically very compute intensive with high communication bandwidth requirements, they are deployed in harsh environments, and they

Figure 1

Many deployed C4ISR systems have to be packaged in conduction-cooled ATR enclosures. The VPX (VITA 46) and OpenVPX (VITA 65) specifications support the design of conduction-cooled boards and systems like this one.

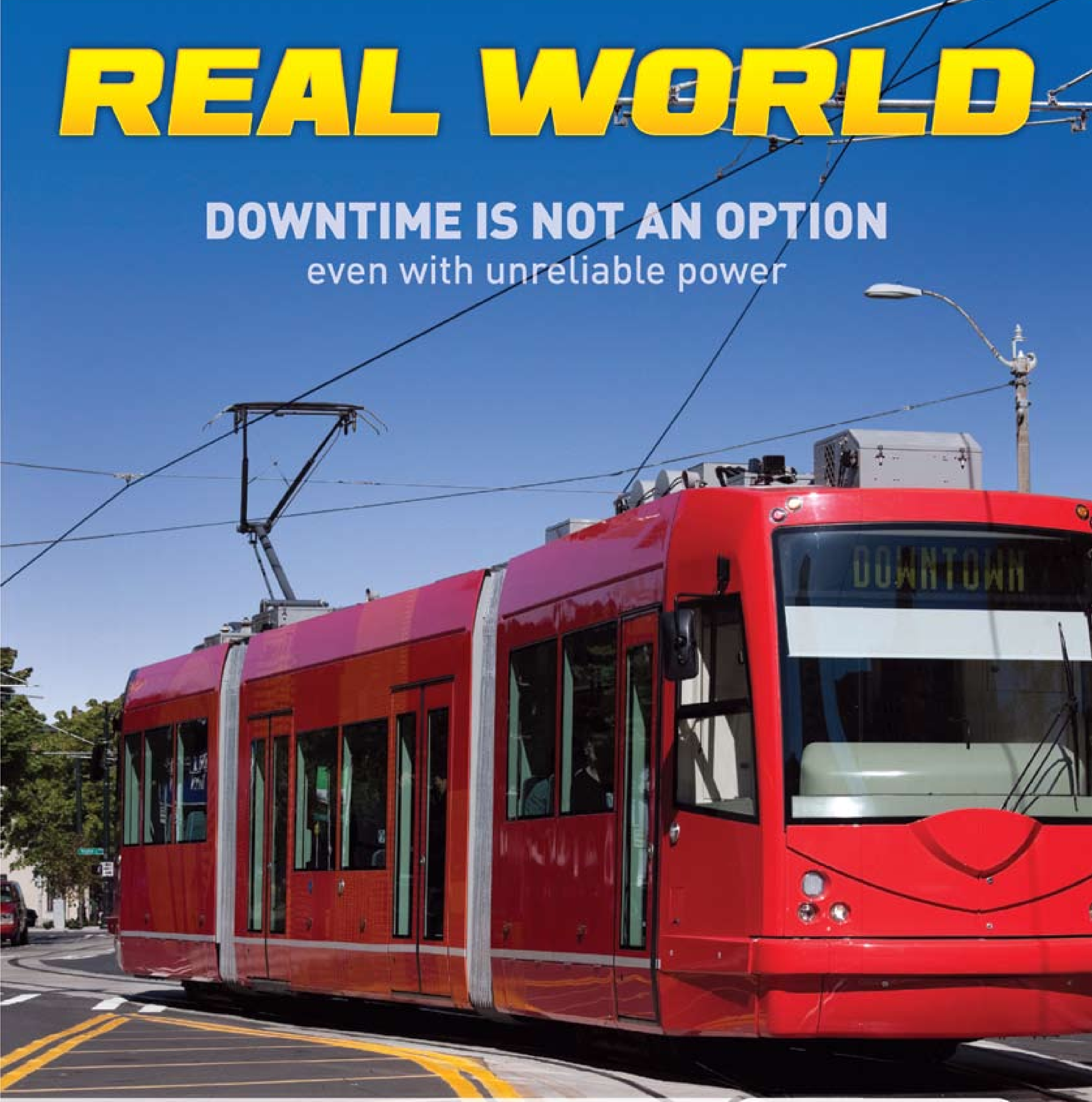
REAL WORLD
DOWNTIME IS NOT AN OPTION
even with unreliable power
DOWNTOWN

Figure 2

For large, high-power systems, air-cooled 6U VPX makes a lot of sense in rack mounted systems for an EP-3 aircraft. The EP-3 aircraft is used for electronic intelligence (ELINT).

have Size, Weight and Power (SWaP) constraints.

C4ISR Apps Push the Envelope

Representative C4ISR applications that have these common attributes are Software Defined Radio, radar processing, threat detection and avoidance systems, mine detection, and target recognition and verification, to name a few. Systems in unmanned vehicles also share these common attributes. A number of ISR systems are being deployed in UAVs and that trend is likely to continue as more unmanned air, sea and ground vehicles move into operation.

This trend to smaller, lighter, faster systems would not be possible without some important technology advances. There are three technology advances in particular that have supported this trend for deployed C4ISR systems. First, switched serial fabric technology has matured to the point where it is an accepted interconnect technology in embedded systems and, in fact, necessary to meet the communications bandwidth requirements in these systems. Fabrics like RapidIO and PCI Express provide multi-gigabyte pipes to move data through a system's data plane while Gigabit Ethernet can be utilized for the control plane communication.

The second advance is processor performance. Processors keep getting faster, but until recently higher performance was equated with higher power consumption to the point where higher-end processors could not be used in many SWaP-constrained applications. With the introduction of processors like the Intel Core i7 processor this has changed. The Intel Core i7 processor significantly increases the performance per watt over previous generations. Increased processor performance is enabling system integrators to deliver capabilities in deployed C4ISR systems that were not possible previously.

The third technology advance is increased device integration. With every generation of processors, more devices are integrated into a one or two chip solution such as memory controllers, PCIe, Gigabit Ethernet, graphics and USB. The drive to integrate more devices into a single chip provides tremendous space savings in systems where board real estate is at a premium.

Multicore CPU Meets Mil Needs

The latest processor from Intel delivers all the technology advances that are driving the trend to smaller, lighter, faster systems. The Intel Core i7 mobile dual-core processor is Intel's latest high-performance processor targeted for the laptop industry. Intel's Embedded Group has acquired this component and enhanced it for the embedded market by incorporating Error Correcting Code (ECC) into the integrated memory controller. Memory with ECC support is a requirement for most military programs as it improves reliability by allowing single-bit memory errors to be corrected and dual-bit memory errors to be detected. Intel's Embedded Group has also extended the standard product life cycle to meet military program requirements.

With the Intel Core i7 mobile processor, Intel has embraced a system-on-a-chip (SoC) design philosophy. This CPU removes the need for a northbridge by integrating a DDR3 memory controller, graphics core and x16 PCI Express interface. By removing the need for a Front Side Bus (FSB) to communicate with these high-performance interfaces, I/O and memory bandwidth are increased significantly. In addition to increasing performance, the SoC approach frees up significant board real estate. While Intel has offered integrated features in the past with their ultra-low-power component line, this is the first case where a high-performance processor and matching high-performance peripherals have been coupled into a single package.

A southbridge companion chip is still present and provides access to additional interfaces including SATA, USB, PCI and additional PCI Express. For applications requiring graphics, such as in-vehicle training systems, DVI graphics is integrated into the processor and southbridge. Integrating DVI graphics eliminates the need for an additional graphics card to lower the SWaP of the system in the vehicle.

In addition to integrating peripheral controllers, Intel has also refreshed the processor's microarchitecture and fabrication process. The performance enhancements of the updated microarchitecture significantly increase floating point and integer capability. Military system developers who currently use the Intel Core 2 Duo processor will see a sizeable performance increase at the same core frequency. The fabrication process improvements allow the core to be run at a lower voltage level, producing a higher performance per watt over previous generations. With the Intel Core i7 processor, Intel has both increased performance while decreasing power consumption. The level of device integration, support for high-speed serial fabrics, and performance per watt make the Intel Core i7 processor particularly well suited for deployed C4ISR applications with size and power constraints.

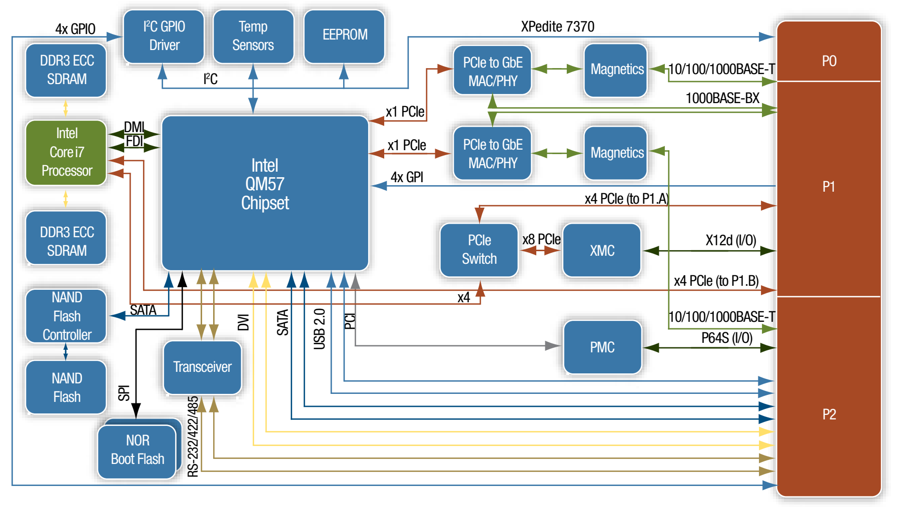

Figure 3

The 2.53 GHz Intel Core i7 processor based XPedite7370 3U VPX SBC will dissipate in the range of 25W to 30W. It offers 4 Gbytes of ECC DDR3 memory, integrated DVI graphics, SATA, USB, PCI Express for the VPX data plane, and Gigabit Ethernet for the VPX control plane.

OpenVPX Supports Next-Gen Needs

As mentioned earlier, deployed C4ISR applications are very compute intensive with high communication bandwidth requirements, they are deployed in harsh environments, and they have SWaP constraints. These systems need to be packaged in such a way that they can withstand the harsh environmental factors such a heat, cold, dust, shock, vibration, EMI and fog. Because of the environmental and SWaP constraints, many deployed C4ISR systems have to be packaged in conduction-cooled ATR enclosures (Figure 1). The VPX (VITA 46) and OpenVPX (VITA 65) specifications support the design of conduction-cooled boards and systems with VPX being the platform of choice for many deployed C4ISR applications.

The advantage of designing a system around the VPX and OpenVPX specifications is that they are accepted standards that support the development of board and system-level components. Board and system-level interfaces and integration issues have been addressed by the standards to provide compatibility and interoperability between boards and system-level components. When contemplating a new design, system designers have the assurance that there is an established ecosystem of VPX building blocks available from multiple embedded computing vendors including SBCs, processing modules, I/O, storage, backplanes, power supplies and enclosures. System integrators can also develop their own VPX boards and system components to integrate with commercial embedded computing components.

VPX supports both 6U and 3U form factors. For large, high-power systems, air-cooled 6U VPX makes a lot of sense, for instance, for a rack mounted system in an AWACS or EP-3 aircraft (Figure 2). But because of the SWaP and environmental constraints of many deployed C4ISR applications, large, air-cooled systems are not an option. For many deployed C4ISR applications, conduction cooling is the only practical choice, and in these instances conduction-cooled 3U VPX is often the right choice. 3U boards have less surface area than 6U boards, which makes 3U boards inherently more robust in terms of shock and vibration.

Reducing Board Count

With the increased level of integration and performance of computer technology, as evidenced by the Intel Core i7 processor, an application that in the past required a rack of 6U boards can now be implemented with a small number of 3U boards. There is a crossover point where more functional density can be achieved by using 6U boards, however, a large number of today's deployed C4ISR systems only need a small number of 3U boards-three to six-and don't reach that crossover point. If the functionality can be accomplished with a small number of 3U boards-such as less than six-it is intuitive that a system built with 3U boards can fit in a smaller space than a system built using 6U boards. Basing a system design on 3U boards also allows for a more modular design.

Cooling is possibly the most important aspect of determining whether to utilize a 3U or 6U form factor for a conduction-cooled, SWaP-constrained design. More functionality can be packed onto a 6U board, however, both 3U and

6U conduction-cooled boards have the same amount of surface area between the wedge locks and the side walls of the chassis from which to transfer heat off of the board.

Even though a 6U board is roughly twice the size of a 3U board, any additional heat it produces has to be transferred across the same heat transfer surface area to the chassis. Without employing exotic cooling methods, which in many cases are not practical, it is not be possible to cool high-powered 6U boards using traditional conduction-cooled approaches. For this reason alone, 3U boards are the better choice for many for conduction-cooled applications.

Tackling SWaP Issues

To minimize SWaP, system designers must maximize the functional density per watt within the given cooling limitations of their system. Traditional conduction-cooling technology can cool up to about 35W per slot. An Intel Core i7 processor-based 3U VPX SBC will dissipate in the range of 25W to 30W. From a thermal standpoint, this class of SBC is perfectly matched with the cooling capabilities of conduction cooling.

By choosing this type of SBC, system designers can maximize the functional density of their systems and thereby achieve the maximum performance in the smallest space. The XPedite7370 3U VPX SBC from Extreme Engineering Solutions (X-ES) (Figure 3), with a processor running at 2.53 GHz, 4 Gbytes of ECC DDR3 memory, integrated DVI graphics, SATA, USB, PCI Express for the VPX data plane, and Gigabit Ethernet for the VPX control plane, is an example of the level of performance and functional density that is possible within this power budget in a 3U form factor.

The Intel Core i7 processor delivers the right features and performance to support compute-intensive deployed C4ISR applications. The form factor of choice for many of these deployed C4ISR applications is conduction-cooled 3U VPX. Combining these two technologies into standard 3U VPX SBCs maximizes functional density for compute-intensive applications. With the available 3U VPX and OpenVPX infrastructure, system integrators have the building blocks they need to develop smaller, lighter, faster systems for their military customers. ▮

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Reaping the Benefits of OpenVPX

Intel Architecture Ups its Appeal for Military Embedded Apps

Once dominated by 68k and Power Architecture-based computing, the military embedded boards market is accelerating its embrace of IA processors. The latest slew Core i7 board rollouts seals the deal.

Jeff Child,
Editor-in-Chief

There used to be a delay—numbered in years—between when the latest and greatest computer microprocessors first rolled out and when they made their way into the embedded computer market, with the military segment jumping on even later. Today that gap is becoming almost non-existent as forces on both the supply and demand side of the equation narrow the gap. On the demand side, more and more advanced military programs are hungry for the very fastest processing solutions they can get while keeping within a constrained power budget. On the supply side, Intel and others have become more accommodating to the needs of long life-cycle markets like the military and sharing design information with the embedded board vendors early.

A vivid example of this trend cropped up earlier this month with Intel's announcement of its Core i7 processor at the International Consumer Electronics Show in Las Vegas. Based on 32nm process technology and the new Intel integrated memory/graphics controller architecture, these processors are from the Intel embedded roadmap, which offers at least seven-year availability. Following immediately on the heels of that, at least seven embedded board vendors announced new SBC products—and in some cases several SBC products—sporting the i7. In the past, the Freescale PowerPC family of processors always had an advantage over Intel's offerings when it came to power dissipation. Freescale meanwhile has kept pace on the performance side with its recent QorIQ P4080 family of processors embedded with up to eight Power Architecture cores.

But now there's no longer a reason to suffer with high power dissipation as a trade-off for using an Intel Architecture platform. And while the PowerPC enjoys a longer legacy in military designs, it's hard to resist the ease of software integration that Intel Architecture platforms allow. Many military system developers these days like to start their development work using Linux and then usually migrate to some kind of RTOS for the deployed system. Taking that route is much more straightforward using Intel-compatible platforms than with others.

Rally Around the Processor

About five years ago, for example, it was obvious that the most prevalent microprocessor designed into new single board computer products was the Intel Pentium M. And then in the past couple years the Intel Core2 Duo has usurped that position as the most designed in CPU on new embedded board products. Now in this current wave of Core i7 board announcements, many of them are on military-oriented form factors.

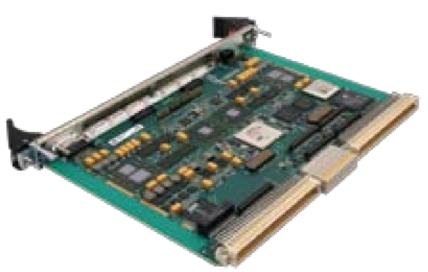

Figure 1

The CHAMP-AV5 serves up a pair of 2.53 GHz dual-core Core i7 processors, and delivers performance rated up to 81 GFLOPs. With a 17 Gbyte/s (peak) DDR3 memory subsystem connected directly to the processor, the Core i7 is able to maximize the throughput of its SSE 4.2 vector processing units.

Extreme Engineering Solutions, along just such lines, this month announced the availability of seven embedded computing products based on the new Intel Core i7 processor across a variety of form factors. All of these products

are available in commercial, air-cooled to rugged, conduction-cooled versions. The ones available immediately include an XMC, a 3U VPX, a 6U VPX and a VME form factor board. These will be followed up in the next couple months with 3U cPCI, 6U cPCI and PrPMC boards based on the Core i7. X-ES's i7 boards make use of the Intel QM57 Express chipset that offers integrated PCI Express, USB, SATA 3.0 Gbit/s and graphics interfaces.

Meanwhile, Curtiss-Wright Controls Embedded Computing has rolled out two i7 offerings. First is a VME64x DSP (Digital Signal Processing) engine using the new dual-core Intel Core i7-610E processor. The second is the SVME/DMV-1905 single board computer, also based on the Core i7 processor. The CHAMP-AV5 (Figure 1) has a pair of 2.53 GHz dual-core Core i7 processors, and delivers performance rated up to 81 GFLOPs. With a 17 Gbyte/s (peak) DDR3 memory subsystem connected directly to the processor, the Core i7 is able to maximize the throughput of its SSE 4.2 vector processing units. With 4 Mbytes of cache and two hardware threads per core, the Core i7 processor can process larger vectors at peak rates significantly greater than was possible with previous AltiVec-based systems.

Figure 2

The Core i7 is even finding its way onto VME for legacy programs and tech upgrades. The rugged 6U VME VR12 is based on Intel Core i7 processing technology and also sports two XMC expansion along with up to 8 Gbytes of DDR3 SDRAM memory with ECC.

Figure 3

The PP 712/08x is a CompactPCI SBC product sporting the Intel Core i7 processor with speeds up to 2.53 GHz. Also on board are up to 8 Gbytes of DDR3-1066 ECC SDRAM, dual PMC/XMC sites and three Gigabit Ethernet ports.

VPX, VME and CompactPCI

GE Intelligent Platforms, for its part, is offering new SBC products based on Intel Core i7 processor technology operating at up to 2.53 GHz. The new boards are the rugged 6U VME VR12 (Figure 2), the rugged 6U CompactPCI CR12 and the 6U VME XVB601. The company also disclosed plans to announce rugged 6U VPX and rugged 3U VPX single board computers based on Intel Core i7 processing technology, making a total of five boards either announced or in development. The VR12 and CR12 also feature the inclusion of two XMC expansion sites in a true single-slot solution, providing customers with access to a broad range of options for I/O, communications and other capabilities. The boards can support up to 8 Gbytes of DDR3 SDRAM memory with ECC.

Emerson Network Power meanwhile has chosen an interesting mix of form factors for their i7 board offerings. The company announced three new embedded computing platforms powered by the latest Intel Core i7 and Intel Core i5 processors. These new embedded computing platforms are available in a range of form factors, including COM Express, MicroATX and 6U VME. Based on the Type 6 COM Express R2.0 form factor (95 by 125 mm), the COMX-CORE-7X0 and COMX-CORE-5X0 feature Intel Core i7 processor 2.0 GHz and 1.06 GHz variants or the Intel Core i5 processor at 2.4 GHz and the mobile Intel QM57 Express chipset. Two SO-DIMM (non-ECC) sockets can accommodate up to 8 Gbytes of DDR3 memory and an optional eUSB flash module extends on-module storage. Connectivity includes one PCI Express x16 and seven PCI Express x1 expansion sockets, one Gigabit Ethernet, four SATA and eight USB 2.0 ports.

Two Independent i7 Nodes

Choosing 6U VPX for its first foray into the Core i7 camp, Kontron introduced the Kontron VX6060, a VPX computing

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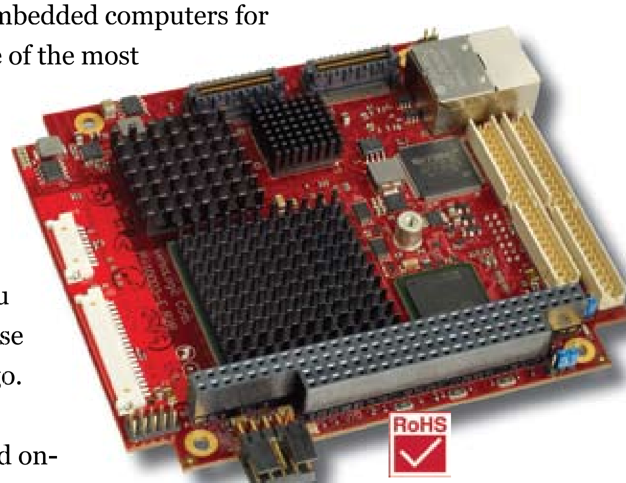

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blade for parallel data and signal processing applications. The board has two independently implemented Intel Core i7 processing nodes linked to a powerful Ethernet and PCIe infrastructure. The board is a useful building block for intensive parallel computing workloads where a cluster of Kontron VX6060s can be used in full mesh VPX or switched OpenVPX environments. Each processing node implements Intel's next-generation high-performance embedded processor with integrated memory controller and Intel HD graphics—the Intel Core i7 processor—coupled with the highly integrated Intel Platform Controller Hub (PCH) QM57 with numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels.

Concurrent Technologies has weighed in with a CompactPCI product sporting the Intel Core i7 processor (Figure 3). Depending on the application requirements, a choice of processors is supported: the 2.53 GHz Intel Core i7-610E, 2.0 GHz Intel Core i7-620LE and the 1.06 GHz Intel Core i7-620UE. With up to 8 Gbytes of DDR3-1066 ECC SDRAM, dual PMC/XMC sites, three Gigabit Ethernet ports, four SATA300 disk interfaces and dual head graphics, the PP 712/08x also offers rear I/O interfaces that are compatible with the popular PP 512/06x family providing a continuing upgrade path. In addition, the PP 712/08x can optionally support extended temperatures ranging from -40° to +85°C.

Even the PrAMC processor mezzanine form factor joined in the game thanks to JumpGen Systems introducing new AMCs based on the Intel Core i7 Processor. The PRM-121 is an AdvancedMC (PrAMC) processor board featuring the 32nm Intel Core i7-620LE processor running at 2.0 GHz and the Mobile QM57 Express chipset with 2 Gbytes of ECC DDR3 memory running at 1066 MHz. The PRM-121 has 2 GigE links and 2 SATA channels routed to the AMC connector.

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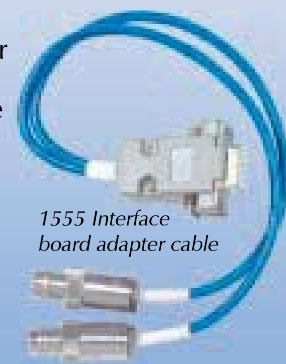

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Case Study: Revving up VPX for 10 Gbaud Operation

Supporting 10 Gbaud data rates is a complex technical challenge. VPX is designed to handle such speeds, but a variety of system design issues must be considered at this level of signal transmission.

Bob Sullivan, V. P. of Technology, Hybricon
Michael Rose, Engineering Consultant, Hybricon
Jason Boh, Applications Engineer, Agilent

VPX has become the de facto standard for the current generation of military embedded computing platforms. These systems include high-speed serial fabrics such as Serial RapidIO, PCI Express, or Ethernet. The initial VPX standards have focused on Gen1 Serial RapidIO, Gen 1 PCIe and XAUI with maximum baud rates of 2.5 to 3.125 Gbaud, Even supporting these rates is not a simple task often requiring a detailed signal integrity analysis and careful attention to the overall loss budget and the numerous signal impairments to ensure success the first time out. The new VITA 65 OpenVPX standard plans to add options for 5 and 6.25 Gbaud as well in order to support Gen2 Serial RapidIO and Gen 2 PCIe.

The recent adoption of IEEE 802.3ap 10GBase-KR, and the availability of silicon transceiver devices from a number of silicon vendors including AMCC, Broadcom and Xilinx, provide the basis for the next increment in VPX performance. This is the first standard communication protocol to support 10Gbaud per pair operation over a backplane, so it is a natural next step for VPX to implement 10GBase-KR for rugged applications. 10GBase-KR will require a signal integrity analysis paradigm shift from the classic time domain approaches (eye diagrams) to frequency domain and statistical approaches. Gen2 Serial RapidIO and Gen 2 PCIe include some of this thinking, but 10GBase-KR takes it to a whole new level.

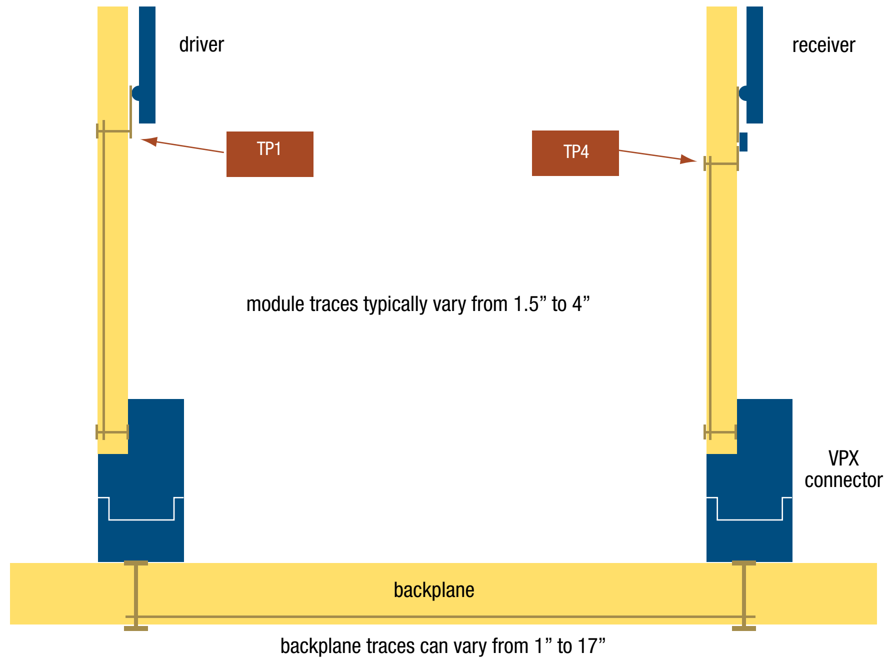

Figure 1

Depicted here is a representative channel topology for VPX REDI with a maximum backplane trace length of 17 inches.

Designing a compliant interoperable channel for 10.3 Gbaud over a single lane on a typical VPX backplane poses a number of technical challenges. To understand these challenges, it’s helpful to looks at a representative VPX channel for 10GBase-KR compatibility using the IEEE 802.3ap compliance metrics. Understanding the tools and techniques for simulating a 10 Gbaud channel is also key.

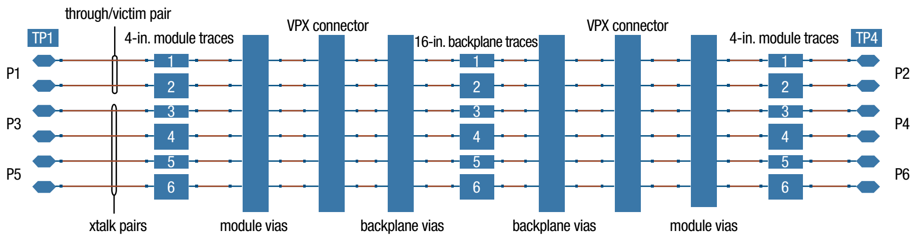

Figure 2

For simulation, the channel topology shown here was constructed as a 6-port mixed-mode cascaded model of the trace sections, the VPX connectors, and their corresponding footprint vias.

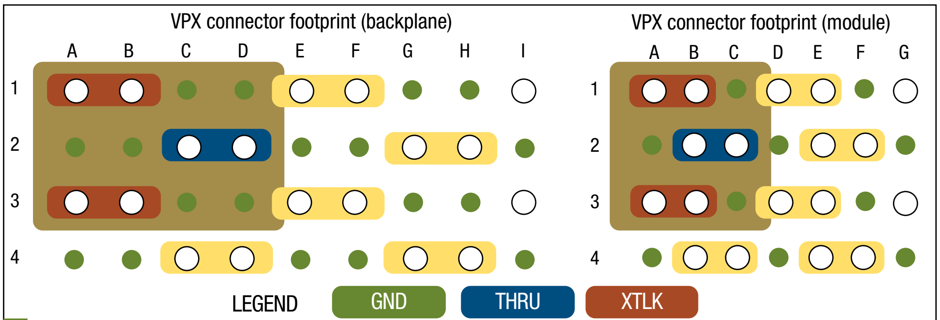

Figure 3

Shown here is a section of a differential VPX connector with the standard pin assignments. The shaded portion of the connector diagram represents the section characterized in the connector S-parameter model.

VPX Channel Topology

VITA 46 systems come in a number of mechanical form factors. Regardless of the chassis arrangement, VPX backplanes are implemented in either 3U or 6U heights. The VPX REDI standards detail the slot pitch (0.8-in., 0.85-in., 1.0-in), the connector footprint and the pin assignments for differential pairs. A representative channel topology is shown in Figure 1. Backplane traces can range from 1 inch for adjacent slots to about 17 inches for a 21-slot, 0.8-inch pitch system. Typically, the maximum trace length is limited to control the maximum attenuation. For this study, we will consider a maximum backplane trace length of 17 inches.

VPX module trace lengths can range from roughly 1.5 inches with the transceiver placed just next to the connectors, to a practical maximum of about 4 inches. In terms of the frequency-dependent skin-effect losses, the module's trace length will often have more impact on the overall channel attenuation than the backplane traces because of the small etch geometries typically used on module PCBs. For this study, we assume that the module does not include a mezzanine connector/PCB in this path.

The IEEE 802.3ap specification defines a compliant channel with specific test point locations. The test channel does not include the transceiver package impairments or the discontinuities related to the BGA escape via or AC coupling capacitors. The test points that define a test channel are noted as TP1 to TP4 in the VPX backplane simulation topology diagram shown in Figure 2.

The 10GBase-KR specifies a number of frequency domain parameters in Annex 69B that can be used to evaluate channel conformance such as fitted attenuation, insertion loss deviation, return loss, and insertion loss to crosstalk ratio. The transmit and receive blocks have their own compliance metrics, which are not simulated or discussed in any detail here. The benefit of a compliant channel is that link performance can be evaluated with the assumption that the transceivers are known to be compliant. This study focuses exclusively on the VPX channel and will use behavioral transceivers integrated into the ADS channel simulation environment to replicate 10GBase-KR transmitter and receiver characteristics.

VPX Connector Modeling

VPX systems based on VITA 46 utilize a MultiGig-RT2 connector; this represents the vast majority of systems in use today. Recently, an alternative Viper connector has become available as well (VITA 60 draft), but it is not in widespread use today. Since the connectors share the same via footprints and pinouts, we will study both of these connectors.

The three-pair VPX connector model used primarily is this study was developed by the vendor using a full-wave EM modeler/solver. Pin assignments for VPX connectors are defined in the corresponding VITA 46 "dot" specification. The current VITA 46.x specification uses a common pin arrangement for differential pairs among all the fabric variants. A section of a differential VPX connector with the standard pin assignments is shown in Figure 3. The shaded portion of the connector diagram represents the section characterized in the connector S-parameter model. The fully coupled 3-pair via models were developed in a full-wave EM solver. Three via cases were developed to evaluate the impact of overall via length and stub length.

Simulation Methodology

The cascaded channel models are swept in the frequency domain in ADS and the behavior is plotted against the limits established in Annex 69B of the IEEE 802.3ap specification. The Annex 69B post-processing equations and limit expressions are implemented directly in ADS. The channel frequency domain model is also converted to time-domain to gain some insights as to the relative impedance discontinuity magnitudes.

Naturally, the largest impedance discontinuity feature of a conventional VPX channel is the connector and its footprint through vias. Dispersions within the connector create crosstalk and mode conversions. VPX backplane connectors have a 1.8 mm pitch which, along with a fairly large footprint via barrel diameter, will typically result in characteristic differential impedance as low as 85 ohms. The contact patch for the press-fit connector pin extends 20-30 mils into the top of the via creating an intrinsic top stub. The length tolerance of the connector pin contact zone effectively limits the depth of back drilling (or blind or stepped via length) and precludes top drilling.

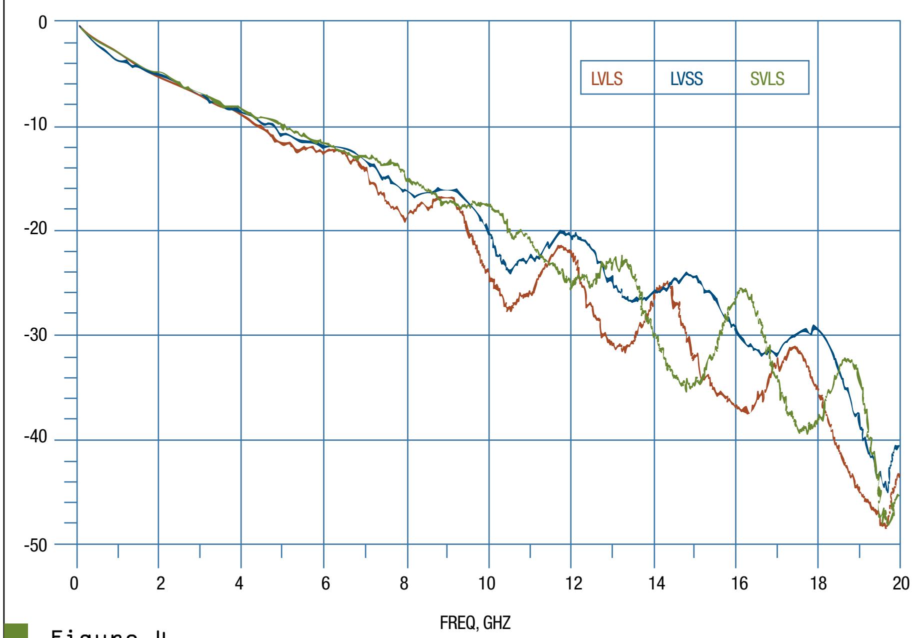

Figure 4

Shown here is channel frequency domain SDD21 for three via cases.

The following VPX connector via cases shown in Table 1 were selected for evaluation because they allow routing on six of the eight available signal layers with a maximum of two levels of back-drilling. Note that in the low-volume, mission-critical VPX marketplace, the costs for back-drilling and low loss dielectric materials can generally be justified.

Channel Frequency Domain Behavior

The good SDD21 and SDD11 performance (Figure 4 and Figure 5) of the overall channel reflects the attention paid to limiting stub length as well as the use of a low loss dielectric material. Differential insertion loss at the Nyquist frequency of 5.156 GHz is in the range of -10.5 dB and -13 dB. The low overall channel attenuation allows designers to consider using less expensive dielectric materials. However, the additional signal-to-noise ratio afforded by the low loss material provides greater crosstalk margins as discussed in the following crosstalk section. This turns out to be an important consideration in meeting 10GBase-KR ICR (insertion loss to crosstalk ratio) limits. Also, the low overall differential insertion loss provides some flexibility for systems with longer trace lengths or more narrow trace widths.

Given the low passband ripple and the relatively low attenuation in the signaling band with the worst-case LVLS configuration, the following frequency domain analyses focus on this via scenario with the exception of the crosstalk evaluation where the via length has a considerable impact on ICR margins. The channel also has good margin to the IEEE 802.3ap recommended return loss limits.

Case	Backplane via length	Backplane stub length	Module via length	Module stub length
Long via / long stub (LVLS)	175	50	115	35
Long via / short stub (LVSS)	150	25	100	15
Short via / long stub (SVLS)	75	40	50	25

Table 1

Listed here are the connector footprint via simulation cases.

Frequency Domain Crosstalk Characteristics

Note that in the VPX differential pair pinout, the C:D pair has two adjacent near end aggressors (E:F pairs) and two adjacent far end aggressors (A:B pairs), so it is a reasonable worst-case pair for crosstalk evaluation. The frequency domain differential NEXT and FEXT crosstalk performance was evaluated using two symmetrical, uncorrelated aggressor pairs acting on the C2:D2 pin pair. The power sums of the individual aggressors were calculated as specified in IEEE 802.3ap, Annex 69B. The PSFEXT and PSNEXT contributions were then power summed to form the overall crosstalk (PSXT).

The architects of the IEEE 802.3ap specification did not define strict crosstalk limits. Instead, acknowledging that some less lossy channels could tolerate higher crosstalk levels, they defined a limit based on the ratio of insertion loss to the total crosstalk (ICR). This measure is analogous to Signal-to-Noise Ratio (SNR). Given the pitch and via barrel diameter of VPX connectors, this measurement method can be of particular benefit in VPX systems. As mentioned above, shorter vias tend to have substantially lower crosstalk. A system designer can trade off the costs of more expensive dielectric materials against a more restrictive routing policy where the 10.3 Gbaud traces are routed exclusively on the top most layers. In the test case, IEEE 802.3ap ICR limits are met with a low loss (dissipation factor of .0075 and 2.5 GHz) dielectric material without introducing the layer routing restrictions mentioned above.

10GBase-KR Equalization

IEEE 802.3ap specifies that transceivers implement, at minimum, 3-tap Feed Forward Equalization (FFE) in the transmitter and acknowledges the probable need for a multi-tap Decision Feedback Equalizer (DFE). Most 10GBase-KR transceivers will implement both FFE and DFE and will likely have a linear equalization stage in the receiver as well.

With three different equalization methods available in most 10GBase-KR transceivers, how is one chosen over another? The worst-case channel described here could be generally characterized as having low attenuation, with low passband ripple, but with only marginal crosstalk immunity. Continuous Time Linear Equalization (CTLE) is not the best choice

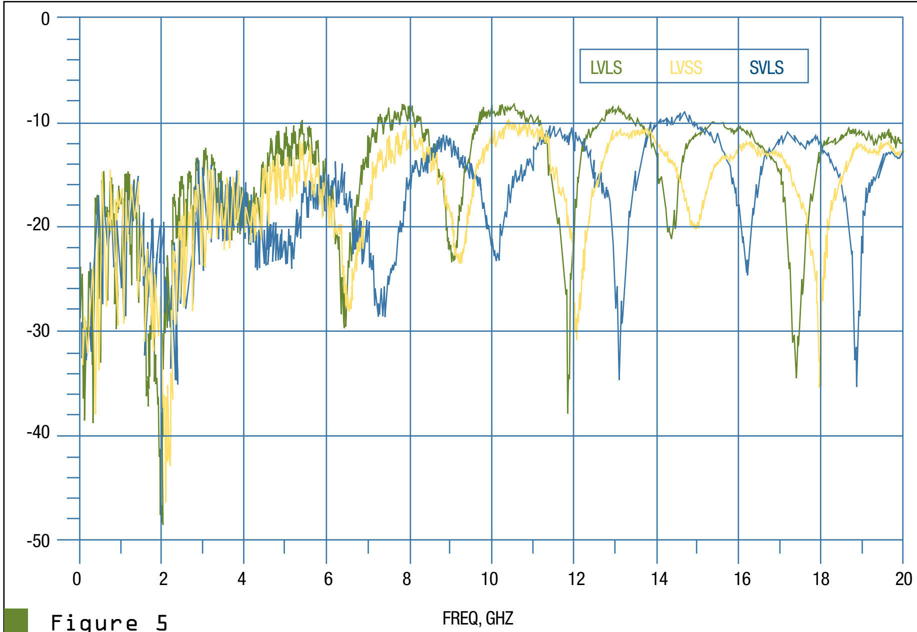

Figure 5

Shown here is channel frequency domain SDD21 for three via cases.

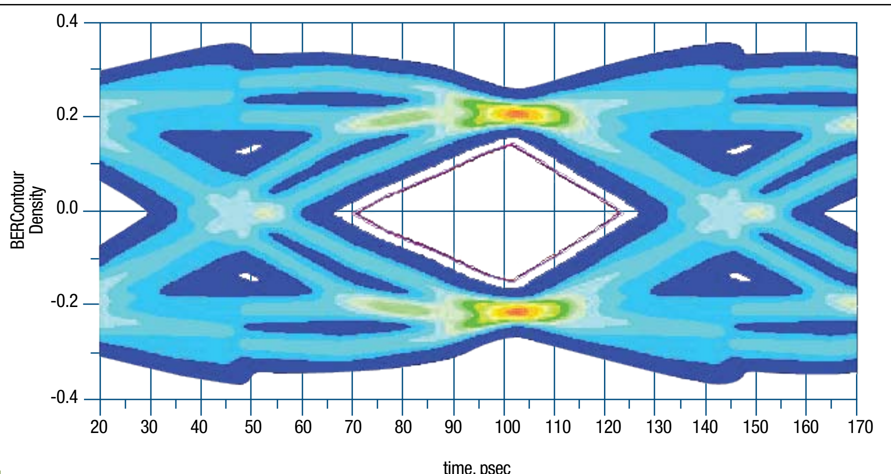

Figure 6

The eye density and contour at BER 10-12 (inner-most opening outline) plots for simulation case 7b of the test.

since the channel is not highly attenuated and linear equalization amplifies noise and crosstalk along with the signal. FFE is an appropriate choice since it provides both pre- and post-cursor equalization.

The number of taps implemented by silicon vendors will vary, but it is probably safe to assume that most will provide at least two pre-cursor and two post-cursor taps. Assuming a limited number of taps, FFE will probably not be able to "reach" the ripple out at the 4.5ns point in the SBR plot. DFE can provide the additional post-cursor equalization. The main draw back with DFE is that it, by nature, will tend to propagate bit errors, especially when the coefficients become large 10GBase-KR defines an optional Forward Error Correction (FEC) encoding sublayer for counteracting multi-bit burst errors. In addition, FEC can improve the effective BER performance of marginal channels.

Equalization Performance

First, eight statistical simulations were performed on just the through channel pair (the crosstalk pairs were just terminated on both ends). The eye density and contour at BER 10-12 (inner-most opening outline) plots for simulation case 7b is shown in Figure 6. The DFE transition responses are evident at zero-crossings. As mentioned earlier, faster rise/fall times will increase the SNR and horizontal opening (at the expense of crosstalk margins and power plane noise coupling). 10GBase-KR specifies a transition time of 24 to 47 pS. At 40 pS, the simulations were performed closer to the worst-case end of the allowable range.

Although VPX is typically operated at 2.5 to 3.125 Gbaud today, the simulations performed indicate that VPX can support the IEEE 802.3ap 10GBase-KR 10.3 Gbaud signaling speed. Advanced, adaptive equalization is the key to obtaining strong, reliable performance despite some inherent limitations of the VPX platform. Mapping 10GBase-KR to VPX requires very careful attention to high-speed design details. The VPX topology simulated in this study is, not surprisingly, sensitive to crosstalk impairments, but with careful attention to via tuning, it is fortunately free of large insertion loss ripple associated with connector-related impedance discontinuities. On more complex topologies, such as modules with transceivers located on a mezzanine card, designers will be faced with some difficult decisions regarding material selection, routing restrictions, spacing rules, trace geometries, and perhaps even connector pin assignments. Designers must pay particular attention to via impairments, both in terms of their overall length and their stub length.

System implementers must come to understand how to best apply equalization on a link-by-link basis. Fortunately, adaptive FFE and DFE equalization methods implemented in current 10GBase-KR transceivers will make this potentially complex task routine. We predict that 10.3 Gbaud interfaces will become as common on VITA 46 platforms as 3.125 Gbaud links are today. The VITA 68 group chaired by Bob Sullivan from Hybricon is currently working to define a VPX compliance channel to allow higher rates on VPX, initially aimed at Gen 2 SRIO and PCIe at 5-6.25 Gbaud, but with an eye toward 10GBase-KR as well.

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James B. Doyle, Congressional Affairs Liaison,
Emerson Network Power Embedded Computing

A significant change in the military equipment market is a shift in focus for equipment development. Electronic warfare driven by C4ISR is gaining favor over big-ticket weapons systems. According to U.S. Secretary of Defense Robert Gates, "The overhaul of the Pentagon's top weapons priorities will orient the U.S. military toward winning unconventional conflicts like the one in Afghanistan rather than focusing on war with major powers." Winning such conflicts requires that both the warfighter and upper command have rapid access to actionable intelligence. And that requires high-performance, data networking.

Ideally, this data networking would operate across the entire force structure so that all service branches could exchange C4ISR information. Further, the networking should operate across multi-national forces. This need for wide interoperability calls for networking solutions that stem from open standards rather than proprietary designs. The ideal solution would be a single architecture that could serve a wide variety of nodes across the services and be able to evolve as application needs change (Figure 1).

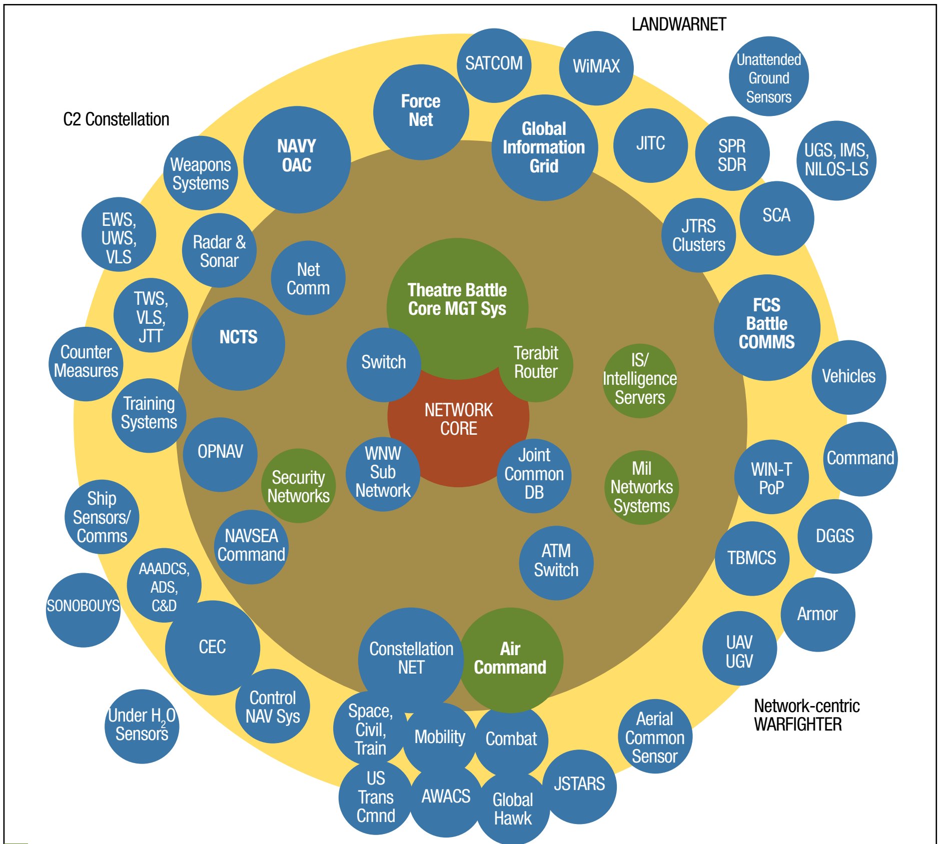


Figure 1

The ideal COTS solution to the military's networking needs would be able to tie together diverse nodes across all service branches.

Application Spectrum

These COTS infrastructures do not necessarily need to handle the extreme conditions of the battlefield, however. Shipboard computing centers, airborne communications platforms and theatre command centers are much more benign environments than field equipment must handle, and equipment for these installations does not need the same extreme levels of ruggedization. The network operations center of a naval vessel, for instance, resides on an isolated deck deep within the ship in an environment similar to commercial IT installations. While this environment is more demanding than that faced by typical consumer electronics, it is not as harsh as that faced by UAVs, tanks, Humvees and the like.

While such installations can use equipment with less than full military ruggedization, they still demand that the equipment provide highly reliable operation. To achieve this, the COTS designs must incorporate high-availability features such as fault tolerance, automatic switchover to redundant systems during hard failures, and support for rapid, hot-swap component replacement. Fortunately, the evolution of the AdvancedTCA or ATCA COTS networking design architecture from its original backplane bandwidth of 1 GbE to the now widely deployed 10 GbE and emerging 40 GbE performance, addresses all of these operational requirements.

ATCA Fits the Bill

The ATCA architecture is an open industry standard originally developed to offer an alternative to proprietary designs in the telecommunications industry. The standard allows multiple vendors to develop individual system components that are interoperable, allowing construction of systems through the mix-and-match of components. The approach is field-proven, with numerous examples of installed ATCA-based systems with more than seven years of operating history.

To meet the industry's operating needs, including compliance to telecom's Network Equipment Building System (NEBS) standards, ATCA was designed from the ground up with a number of key features, all of which are applicable to the military's requirements. The architecture is modular, allowing considerable functional diversity to arise from the assembly of relatively few component pieces. The architecture is also highly flexible, supporting a wide variety of networking standards over a configurable serial backplane.

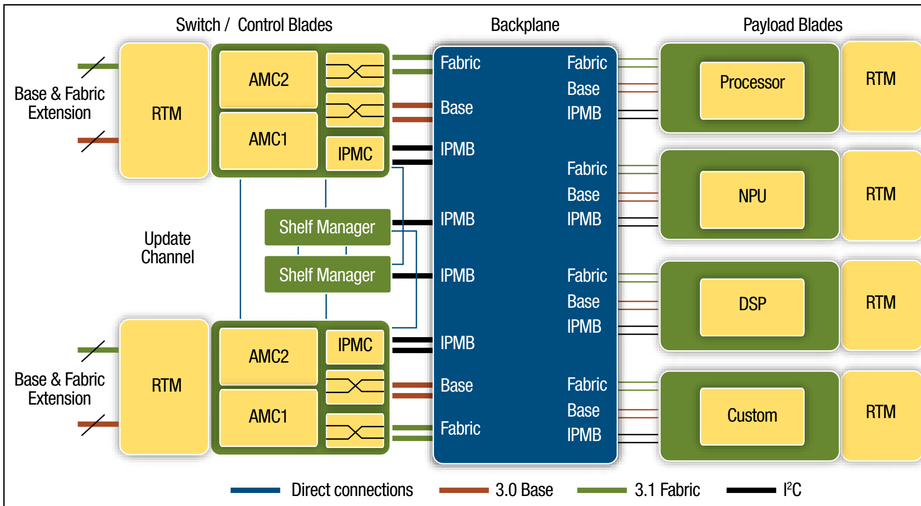


Figure 2

ATCA includes a built-in system management function that provides the essential features of fault-tolerant, high-reliability system design, as illustrated by the architecture of the Centellis 4440 40 Gbit-ready ATCA system platform.

The ATCA architecture is also more robust than typical industrial computing structures. ATCA targets high-reliability installations with specifications that require built-in support for live insertion and hot swap of modules and boards as well as system components such as power supplies and cooling fans. Fault detection and system control are built in, allowing module-level isolation and replacement as well as support for failover operation when using redundant designs. Even the system software targets high reliability, with a robust real-time operating system and high-availability middleware available as a standard software base.

ATCA specifications also call for system operation in harsher environments than the typical home or office. Because telecommunications equipment must often run unattended for months at a time in tight quarters such as small cinder-block buildings, the ATCA specifications call for operation at sustained temperatures as high as 55°C, with the ability to maintain operation for several hours even in the event of failures in the cooling system. For shock and vibration, the specifications require that equipment survive and continue functioning through a major earthquake.

ATCA Structure

A high-level look at the ATCA architecture reveals how it achieves these goals. The basic building block of an ATCA system is the blade, which inserts into a high-speed switched serial backplane. Each blade has access to as many as 21 serial channels, called lanes, with each lane handling data at rates as high as 12 Gbits/s. This gives a combined data throughput capacity of 2.4 Terabits/s for an ATCA system.

The switched-serial backplane is protocol-agnostic allowing it to support a variety of serial communications formats, including 10 Gbit Ethernet (10 GbE), Serial RapidIO and PCI Express. An ATCA backplane can support virtually any serial connection to outside equipment in its native format and provides guaranteed bandwidth for inter-blade communications.

The appeal of Ethernet-based networking in the digitized battlefield is clear. And with the advent of 10 GbE and beyond, Ethernet is no longer limited to the command and control fabric in systems. It can also function as a "fat pipe" that reaches all the way down to high-bandwidth sensors. With that in mind, it's not surprising that 10 GbE is being designed into more and more defense applications, both in the main network and as the pipe to and from sensors or effectors.

Figure 3

Tests by Northrop Grumman demonstrated that ATCA equipment is able to survive "barge testing," showing its suitability for deployment as shipboard systems. MIL-S-901D Heavyweight Shock Test. (Photographs courtesy of National Technical Systems in Rustburg, VA.)

10 GbE-based ATCA systems can also support a wide range of military, aerospace and government applications including sophisticated adaptive beamforming for satellite communications, test equipment with multiple processing elements, long-range radar systems, and high-bandwidth, low-latency wireless test beds.

System Management

An integral part of an ATCA system is its built-in system management (Figure 2). Each ATCA blade or AMC module on an ATCA blade communicates with a shelf manager for monitoring, setup and control. Other field-replaceable units, such as cooling units and power modules, also have management controllers.

The management controllers have the ability to determine module type for electronic keying. They can also detect failures and shut down their client's operation to prevent a single failure from affecting system operation. AMC modules, for instance, have independent power connections for the MMC and the rest of the module, with the MMC having control over the I/O drivers on the AMC. This allows the MMC to disconnect the AMC from the system backplane and power it down in the event of failure or the need for hot-swap replacement. Similar capabilities are built into the cooling units and power modules. Higher-level software can use this infrastructure to implement such functions as failover to redundant hardware for high-availability operation.

ATCA Ecosystem

The goal behind the creation of ATCA was to give networking equipment providers a robust alternative to proprietary designs to both speed development cycles and reduce cost while maintaining the ability to implement product differentiation. Fulfilling that promise required the creation of a robust COTS ecosystem to provide multiple sources for system components while ensuring interoperability among the offerings. This ecosystem is now both substantial and well established.

The PCI Industrial Computer Manufacturers Group (PICMG) developed and maintains the ATCA standard, including definition of chassis, modules, boards and system management operation. More than 60 companies belong to PICMG and provide a wide range of ATCA blades, AMC modules, chassis and full systems. This diverse supplier base not only gives developers multiple sources for many system components, it allows developers to choose the best in class for each component. The Communications Platform Trade Association (CP-TA) provides definitions and test procedures to ensure thermal and system management interoperability among these ATCA products. Other industry organizations provide standards and reference implementations for operating systems and high-availability middleware.

In addition to its telecommunications origin, ATCA has also proven itself in applications such as medical systems, enterprise data centers, financial systems and the military. For example, an ATCA-based system is currently providing ISR support in the Multimission Maritime Aircraft (MMA) system. Systems based on ATCA are also under evaluation for programs such as CANES (Consolidated Afloat Networks and Enterprise Services). Northrop Grumman recently performed afloat shock testing, better known in the defense industry as "barge testing," on two Emerson Network Power ATCA systems to verify their continual operation in a shipboard environment throughout a blast scenario (Figure 3). The equipment showed no faults over a series of tests involving multiple blasts and a variety of equipment mounts and orientations.

ATCA Roadmaps

Along with being a proven architecture, ATCA is continually evolving to take advantage of new technologies as well as expand its application range. The modular nature makes upgrades of processors and adding new interfaces relatively simple. The architecture itself is also seeing upgrades through the continual efforts of the PICMG organization, which has established a new subcommittee to develop the standard—named ATCA Extensions.

The brief for ATCA Extensions is fairly wide-ranging, encompassing from simple changes to make existing blades more cost-optimized for non-central office environments through to supporting new higher compute density system configurations including double-wide server blades to make use of bigger heat sinks to further increase CPU power and back-to-back enclosures to make more use of typical data center rack depths. However, backward and forward compatibility remain key driving principles, preserving existing investment and the ability to make use of other components in the ecosystem to arrive at the best solution.

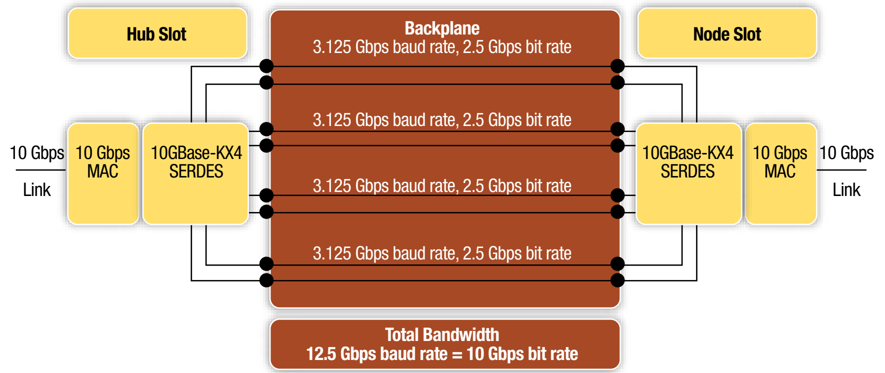


Figure 4

The current ATCA specification allows the combination of four lanes to provide a 10 Gbit/s link between boards, and specifications are under development to extend this to achieve 40 Gbit/s.

ATCA backplane speed increases are also under development. The PICMG organization has already adopted an approach for providing a 10 Gbit/s serial channel across the backplane using four 2.5 Gbit/s lanes operating together. It is now developing new specifications for connectors and backplanes that would allow the same structure to utilize 10 Gbit/s speeds on those four lanes to create a 40 Gbit/s channel (Figure 4). In anticipation of this specification, Emerson Network Power is now offering chassis systems that are "40 Gbit/s Ready" to simplify system upgrade when corresponding blades and AMC modules become available.

Such development efforts by the PICMG organization reflect a commitment within the ATCA ecosystem to continually improving the specification and keeping abreast of new technology opportunities. For military applications, this commitment translates to assurances that ATCA-based systems will be upgradeable to track the state of the art for many years to come. Routine upgrades can be handled through module and blade replacement and, while major upgrades may occasionally require chassis replacement, blades and software should remain compatible across most such replacements.

ATCA Fit for Duty

The ATCA architecture thus meets all the key criteria for COTS-based military system designs. It is designed specifically for high-availability applications in moderately harsh environments similar to many military infrastructure installations and is undergoing extensions to add ruggedization options for even harsher environments. Its modularity gives it the flexibility to adapt to a wide variety of data protocols and I/O interfaces, while simplifying maintenance and supply by minimizing the number of building blocks needed across multiple system designs.

The ATCA system design approach is proven, and has already demonstrated itself in both commercial and military applications. Because it is based on an open standard, ATCA has the support of a large and well-established ecosystem of vendors and industry organizations, including those dedicated to ensuring interoperability among multi-vendor products. This makes it an ideal platform for system developers seeking rapid development at low cost. Further, the flexibility of the architecture gives ATCA the ability to meet many different military networking needs, helping ensure interoperability among diverse systems for information exchange and avoiding "stovepipe" installations. ▮

Emerson Network Power
Tempe, AZ.
(800) 759-1107.
[www.emersonnetworkpower.com].

Technology Focus

Serial FPDP Boards

FPDP Boards Maintain Niche in High-Bandwidth Apps

FPDP offers a straightforward, low-overhead interface scheme for high-bandwidth, point-to-point data movement applications like radar and sonar.

Jeff Child,
Editor-in-Chief

Many kinds of high-performance embedded computing systems in the military market have an appetite for high-speed data from sensors. Often such input is presented as one or more channels of analog data, and in some cases, the sensor data is provided directly to the processing system. However, in other cases, the sensor data is converted to digital data by a smaller system near the sensor itself and then sent over one or more fiber optic links to the processing system. For these applications, Serial Front Panel Data Port (FPDP), or ANSI/VITA 17.1-2003, provides a simple point-to-point protocol with low overhead, high throughput and minimum latency.

Serial FPDP overcomes a key limitation of parallel FPDP: its distance limitations. It does so by using a serial interface based on the Fibre Channel physical layer. Serial FPDP retains the frame format of the original standard thus simplifying the exchange of data between parallel and serial implementations. As a result, Serial FPDP makes it easy to exchange data from local chassis and legacy systems using parallel interfaces to remote chassis through a Serial FPDP connection.

When Serial FPDP was originally deployed, it was based on the fiber optic transceivers that were readily available at the time. The fastest version of Serial FPDP uses a bit rate of 2.5 Gbaud, providing 247 Mbytes/s after 8B/10B encoding. As sensor technology improved, the sensor-to-processor interface often combined multiple Serial FPDP links to meet the ever increasing need for bandwidth. Although this approach provides the necessary throughput, it adds complexity at both ends of the link to manage splitting the data at the source and then aligning the resulting fiber optic streams at the destination. Because there is no standard method for doing this, link aggregation becomes an application-specific part of the problem.

The latest version of Serial FPDP, VITA 17.2, addresses these requirements in two ways. First, the choices for raw bit rates are expanded to include 3.125, 4.25, 5.0 and 6.25 Gbaud, allowing each link to operate up to 2.5x faster than before. Second, the standard now includes the capability to aggregate links in sets of 1x, 2x, 4x, 6x, 8x or 12x, allowing a single logical link to consist of multiple underlying physical links. The net result is that a stream of sensor data of up to 75 Gbaud (7.5 Gbytes/s) can now be considered a single Serial FPDP link.

Figure 1

One of the Littoral Combat Ship's (LCS) mission packages is mine warfare (MIW). The MIW module includes the AN/WLD-1 remote minehunting system, along with other mine detection gear.

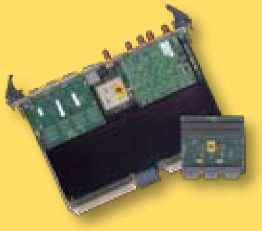
Sonar is among the key applications that have used FPDP, including such major sonar upgrade programs as the SQQ-89 sonar upgrade for the guided missile (DDG) class of destroyers, the sonar for the New Attack Submarine (NSSN) and the P3 Aircraft. The SQQ-89 Sonar transmit and receive systems are used on Arleigh Burke Class (Aegis) Guided Missile Destroyers. The sonar suite aboard the vessel class is the Lockheed Martin SQQ-89(V)6, which includes Edo Corporation AN/SQS-53C bow-mounted active search and attack sonar and the AN/SQR-19B passive towed array. The suite was upgraded to SQQ-89(V)15 to allow deployment of the Lockheed Martin AN/WLD-1 Remote Minehunting System (Figure 1).

Technology Focus:

Serial FPDP Board Roundup

VME Card Provides 24 Serial FPDP Channels

Using FPGAs in conjunction with the Serial FPDP (sFPDP) interconnect makes for a powerful combination. Such a solution has enormous benefits for radar, sonar, SIGINT, ELINT, digital signal processing, FFTs, communications, software radio, encryption, image processing, prototyping, text processing and other processing-intensive applications. Serving exactly that arena, Annapolis Micro Systems offers its FPGA-based WILDSTAR family that provides 24 sFPDP channels per VME slot. The Annapolis sFPDP Cards (UNI3 or UNI6) come with an easy-to-use Serial FPDP interface supporting up to 12 lanes of 2.5 Gbit Full Duplex data. Three frame types are supported: Normal Data Fiber Frame, Sync without Data Fiber Frame and Sync with Data Fiber Frame in Point-to-Point Mode. The card has three individually configurable, industry-standard 4X connectors, providing 4 lanes per connector, with dedicated signal conditioners to ensure clean communication. It supports up to 7.5 Gbytes/s full duplex per I/O card and a wide variety of readily available copper and fiber cables.



Up to two serial I/O cards and two LVDS I/O cards can reside on each WILDSTAR 4 or WILDSTAR 5 VME/VXS main board, with half that number for the PCIX or PCIe. The sFPDP card (UNI6) also supports Rocket I/O protocol at up to 75 Gbit Full Duplex per I/O card, three ports of 10G Full Duplex InfiniBand per I/O card or 10G Full Duplex Ethernet per I/O Card. WILDSTAR 4 for PCI boards starts at about $13,500 and UNI6 I/O Mezzanines start at about $4,500.

Annapolis Micro Systems
Annapolis, MD.
(410) 841-2514.
[www.annapmicro.com].

Board Serves 3.125 Gbits/s on Four Ports

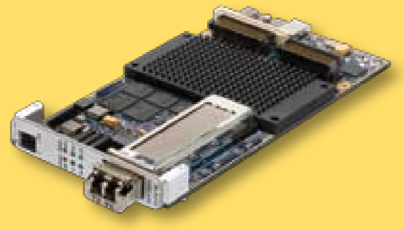
It's not always possible to get data conversion gear close to where the analog data is acquired. Serial FPDP is rapidly becoming the interconnect of choice for streaming data capture systems because it is a protocol optimized for maximum data rates and minimum overhead. It efficiently accommodates many applications requiring great distances between the data input site and data processing stations. Along those lines, Conduant offers its StreamStor Serial FPDP Mezzanine Board for long-distance, high-speed data capture from Serial FPDP or other optical fiber data protocols. When combined with Conduant's StreamStor Amazon SATA disk controller, real-time data input performance exceeds 500 Mbytes/s.

The StreamStor Serial FPDP Mezzanine Board features four independent optical fiber interface ports for simultaneous data input and output available on each port. With data rate and wavelength options, the board can support cable lengths up to 25 kilometers. The StreamStor Serial FPDP Mezzanine Board exceeds the ANSI/VITA 17.1-2003 specification with sustained rates of 300 Mbytes/s (3.125 Gbytes/s). Wavelength options include 850 nm (nanometers) and 1300 nm for distances up to 25 kilometers. Data rates range from 1.06-3.125 Gbits/s on each of the four ports. The mezzanine board supports multiport recording whether bonded or independent. It is field-upgradeable and features customizable hardware.

Conduant
Longmont, CO.
(303) 485-2721.
[www.conduant.com].

XMC Does Sensor I/O over Ethernet, FPDP

The military has warmed completely to the idea of using Ethernet as high-performance interconnect technology. Its ubiquity and longevity make it hard to resist. Applying Ethernet to wide-band sensor I/O, Critical I/O has announced SensorLink, a board-level solution that allows wide-band sensors to be easily connected to, and managed over, 1 Gbit and 10 Gbit Ethernet networks. SensorLink enables system designers to implement an Ethernet "Sensor Fabric" for high-performance systems. The FPGA-based board is a fully self-contained sensor-to-10 Gbit Ethernet bridge. It bridges multiple parallel sensor data ports-that can be configured as industry-standard parallel FPDP and FPDP II, high-speed parallel LVDS, or PCIe-to standard 1 Gbit or 10 Gbit Ethernet, without the need for any host processor at the sensor.

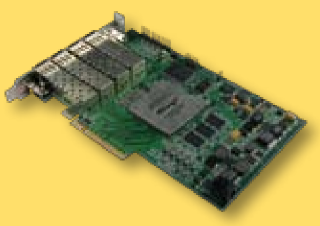


With SensorLink, Ethernet data networks can be applied to even the most demanding real-time applications such as radar, data acquisition, sonar, FLIR, SIGINT, video distribution and signal processing. Completely self-contained and requiring no host processor, SensorLink allows sensor data to be streamed at wire speed with very low latency to other devices connected to the Ethernet network such as signal processors, workstations, storage devices or other SensorLink devices. SensorLink also greatly simplifies the management of sensors by allowing remote processors to configure, control and monitor them through the same Ethernet connection without interrupting the sensor's real-time data flow. SensorLink allows system developers to directly leverage standard Ethernet networks without investing many man-years in software and compatibility testing.

Critical I/O
Irvine, CA.
(949) 553-2200.
[www.criticalio.com].

Quad Channel Serial FPDP Board Is FPGA-Based

The Serial Front Panel Data Port (sFPDP) interconnect has become the industry standard for high-speed serial communication in today's advanced sensor-to-DSP systems. For its latest sFPDP offering, Curtiss-Wright Controls Embedded Computing has introduced a new rugged, high-performance, quad channel Serial FPDP card that delivers sustained data rates up to 247 Mbytes/s on each of its four channels. The new FibreXtreme SL100/SL240 Serial FPDP card, based on Altera's Stratix II GX FPGAs, connects distributed devices through a highly specialized communications protocol (VITA 17.1-2003) optimized for maximum data throughput. The Stratix II GX FPGA is used to obtain full throughput rate on all four sFPDP channels while providing a full rate PCI Express host bus interface. The embedded transceivers in the FPGA support data rates in excess of 6 Gbits/s, enabling future performance enhancement.

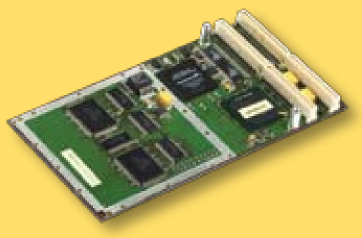


The cards, available in both PCI and XMC mezzanine formats, are designed for use in applications that require high data rates such as digital signal processing, radar and sonar, medical imaging, range and telemetry systems. The sFPDP card off-loads the host processor, enabling data transfers to occur without the CPU overhead and non-deterministic latencies associated with many layers of complex software protocols.

Curtiss-Wright Controls
Embedded Computing
Leesburg, VA.
(703) 779-7800.
[www.cwcembedded.com].

Rugged PMC Supports FPDP II Transmit and Receive

Demand is on the rise for multichannel, high-rate sensor data transfer across a single backplane. Providing a solution, GE Fanuc Embedded Computing offers the ICS-8500, the first PMC to become available that delivers 400 Mbyte/s FPDP II-compared with 160 Mbytes/s for FPDP-in a rugged environment. The ICS-8500, which can be configured as either a transmitter or a receiver, also features 8 Mbytes of swing buffer memory, setting it apart from products that provide only limited FIFO capability.



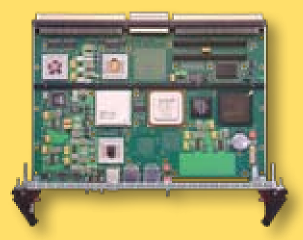
Available in convection- and conduction-cooled versions, the ICS-8500 offers similar functionality to the popular ICS-500-R and ICS-500-T PMC products, but is configurable under software control as either a receiver or transmitter. The 400 Mbyte/s FPDP II interface is provided via the P4 connector: when the ICS-8500 is communicating with a non-FPDP II device, it automatically reverts to ANSI/VITA 17 FPDP operation at 160 Mbytes/s.

In transmit mode, the board provides an FPDP/TM interface. In addition to a continuous data transmit capability, a Loop mode of operation is available in which a fixed length of data equal to the programmed buffer length is written to both banks of the swing buffer. When triggered, this data is repetitively generated and transmitted by the FPDP output interface. In receive mode, the board provides both Receive (FPDP/R) and Receive Master (FPDP/RM) capabilities. A key feature of the product is its ability to perform the corner turning function: this software-enabled feature reorders multichannel data from "channel ordering by time" to "time ordering by channel."

GE Fanuc Intelligent Platforms
Charlottesville, VA.
(800) 368-2738.
[www.gefanucembedded.com].

RapidIO and Serial FPDP Team up on VME Blade

Intensive signal and data processing systems such as radar and imaging equipment, place high demands on high-performance, low-latency throughput. Feeding such needs, Kontron offers its PowerNode5, the first dual 64-bit PowerPC970 VME blade server with backplane Serial RapidIO and Serial FPDP connectivity. The board is a rugged 6U VME PowerPC blade server featuring two 64-bit PPC970s running at 1.6 GHz. Its design is a clone of the IBM JS20 blade computer, providing the PowerNode5 with a very high level of performance and full binary compatibility with IBM JS20 blade servers, in a 6U form factor fully adapted to any of today's embedded systems requirements.

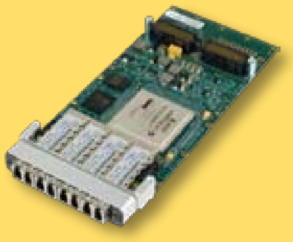


Kontron's Serial RapidIO switch fabric is an original implementation with a distributed Serial RapidIO architecture: each PowerNode5 is equipped with a 4-port switch allowing a flexible, full-mesh interconnect of up to four PowerNode5s and scalable up to a 16-PowerNode5 machine. The PowerNode5 features triple x4 Serial RapidIO links available on an enhanced performance P0 connector, compliant with legacy VME64x backplanes. The PowerNode5 is also available with a twin Serial RapidIO link plus a single Serial FPDP link option. The current version of the PowerNode5 blade computing node is currently shipping with an entry-level unit price of $9,670.

Kontron America
Poway, CA.
(858) 677-0877.
[www.us.kontron.com].

XMC Card Marries RapidIO and sFPDP Streaming I/O

The Ensemble IO Mezzanine Series IOM-120 and IOM-140 (IOM-1x0) sFPDP XMC from Mercury Computer Systems brings enhanced performance and flexibility to external I/O in a serial-based XMC (Switched Mezzanine Card, VITA 42.2-2006). Providing 2.5 Gbaud of full-duplex bandwidth per channel and two or four channels per card, the IOM-1x0 Module offers high levels of speed and connection density.

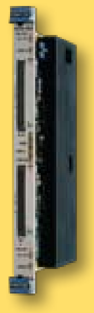


With fiber connection distances of up to 150m and latency as low as 4 ìs, the IOM-1x0 Module is ideally suited as the real-time digital interface for sensor input or data output in a serial RapidIO system. The IOM-1x0 Module implements the Serial Front Panel Data Port (sFPDP) protocol, as specified by VITA 17.1-2003. It supports all four sFPDP framing modes. This implementation of the standard makes the IOM-1x0 Module compatible with products supporting any subset of the VITA 17.1-2003 protocol. The module is software-compatible with RACE++ Series RINOJ-F products, easing migration from the legacy I/O daughtercards, while offering significant improvements in speed and configuration flexibility. The IOM-1x0 Module is more than an ordinary digital interface: each channel can be programmed for data distribution without processor intervention. The interface can sense signals in the input data stream that indicate sensor mode changes and route data appropriately for each mode. Each mode can be made to correspond with an application-defined direct memory access (DMA) command packet (CP) chain. These command packets cause the channel's DMA controller to route the data to a predefined destination anywhere within the RapidIO switch fabric.

Mercury Computer Systems
Chelmsford, MA.
(978) 256-0052.
[www.mc.com].

Data-Capture and Processing Board Samples at 2 GHz

Signals in the 900 MHz range require some power processing to digitize. In the past it's been nearly impossible to directly digitize signal bandwidths up to 900 MHz, in order to capture wideband radar and communication signals as a single channel instead of digitizing several smaller bandwidth slices. Pentek has smoothed the way with its Model 6826 VME A/D Converter board. The Model 6826 features single- or dual-channel data acquisition at a blazing 2 GHz samples/s with 10-bit resolution using the new Atmel AT84AS008 A/D device. The inclusion of the Virtex-II Pro FPGA is essential for processing these large bandwidth signals to extract information and reduce the data rates to a manageable level within the system. The board's ability to accept either single-ended or differential inputs preserves signal integrity across a variety of analog signal sources.



The Model 6826 also features extensive memory resources. Dual 64-bit, high-speed DDR SDRAMs provide a total of 512 Mbytes or 1 Gbyte of memory to store raw data in transient-capture mode. To support high-bandwidth data capture, the board includes several high-speed I/O channels to move the raw data off-board for storage or processing. Two or four channels of FPDP-II data ports, operating at up to 400 Mbytes/s each, deliver processed and de-multiplexed data through legacy connections to other VME cards. In addition, the board offers two serial switched-fabric VXS connections, each running full duplex at 1.25 Gbytes/s to support the new Xilinx Aurora, Serial RapidIO and PCI Express protocols. LVDS I/O is also available on either front or rear panel connections.

Pentek
Upper Saddle River, NJ.
(201) 818-5900.
[www.pentek.com].

25.6 Gbit/s Bandwidth Delivered on sFPDP PMC/XMC

Raw, full-out bandwidth is what FPDP is all about. With that in mind, TEK Microsystems' JazzFiber-V5 Serial Front Panel Data Port (FPDP) I/O module features high-performance streaming sensor I/O interfaces. The JazzFiber-V5 module provides single and multichannel ANSI/VITA 17.1-2003 Serial FPDP interfaces with the hardware, firmware and software features to support the emerging VITA 17.2 standard for Serial FPDP extensions.

The JazzFiber-V5 module is the first Serial FPDP I/O module to support four fiber optic interfaces at up to 6.4 Gbits/s for aggregate throughput of 25.6 Gbits/s. It uses the latest Virtex 5 FPGA technology, including FXT devices. The card does classic Serial FPDP plus draft VITA 17.2 extensions, including channel bonding, higher bit rates and protocol enhancements. The card sports 512 Mbytes of DDR3 memory with 6.4 Gbytes/s of onboard throughput. The module will support memory capacities of up to 2 Gbytes when higher density memory devices are available.

The PMC interface is a PCI-X 64-bit 133 MHz local bus. The XMC interface is PCI Express 1.0a x8 for 2 Gbyte/s full duplex throughput. Commercial, rugged air-cooled and rugged conduction-cooled options are available. The integrated firmware and software transparently support single Serial FPDP streams as well as logical streams using x2 and x4 channel bonding defined in VITA 17.2.

TEK Microsystems
Chelmsford, MA.
(978) 244-9200.
[www.tekmicro.com].

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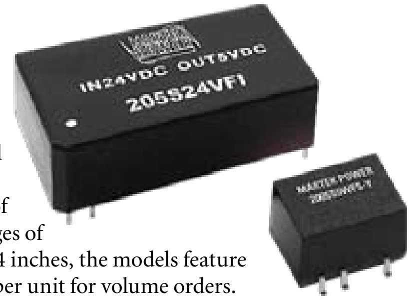


2W DC/DC Converter Pair Boast Miniature Packages

SWaP (Size, Weight and Power) has become a top priority in many of today's military designs. Helping with that, Martek Power has announced two new series of compact DC/DC power converters. The 200VFI and 200WFRS series are specially designed to address the application needs for data communication equipment, mobile battery-driven equipment, distributed power systems and robotic systems. The 200VFI series is a family of cost-effective 2-watt single and dual output DC/DC converters with 18 models that operate from input bus voltages of 5V, 12V and 24V; producing output voltage levels of 5V, 12V, 15V, ±5V, ±12V and ±15V. Measuring 1.25 x 0.8 x 0.4 inches, the models feature short circuit protection, 4000 VAC input/output isolation and built-in PI filter. The 200VFIs are priced at $11.75 per unit for volume orders.

Also new is the 200WFS series of cost-effective 2-watt single and dual output DC/DC converters in an ultra-miniature "gull-wing" SMT package. Thirteen models operate from input bus voltages of 5V, 12V and 24V; producing output voltage levels of 5V, 12V, ±5, ±12V and ±15V for a wide choice. With many standard features such as 1000 VDC input/output isolation, 2:1 Input range and remote on/off control, the units are priced at $6.50 per unit for volume orders.

Martek Power, Torrance, CA. (310) 202-8820. [www.martekpower.com].

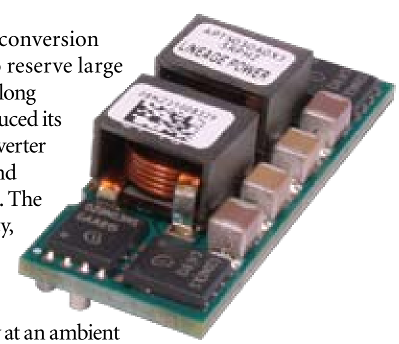
Debug Solution Supports ARM Cortex-A8 Processors

Finding tricky hardware bugs in a military embedded system has always been an X-factor in terms of time and effort. Making that task easier, Macraigor Systems has ported their proprietary On-Chip Debug Technology (OCDemon), GNU Tools Suite and Eclipse Ganymede/Galileo platform to the ARM Cortex-A8 processor. The Cortex-A8 is ARM's first superscalar processor featuring technology for enhanced code density and performance, NEON technology for multimedia and signal processing, and Jazelle RCT (Runtime Compilation Target) technology for high-performance, power-efficient mobile devices.

The Macraigor Eclipse Ganymede/Galileo + GNU Tools Suite is an implementation and packaging of the Eclipse Ganymede/Galileo platform, CDT (C/C++ Development Tooling) 5.0.x and DSDP (Device Software Development Platform) 1.0 plug-ins, and a program called OcdRemote that provides an interface between Eclipse, the GDB debugger and a Macraigor On-Chip Debug device. OCDemon for the ARM Cortex-A8 is available immediately starting at $250. The port of the GNU Tools Suite and Eclipse Ganymede/Galileo platform is being offered at no charge and can be downloaded at www.macraigor.com.

Macraigor Systems Brookline Village, MA. (617) 739-8693. [www.macraigor.com].

30 Amp POL DC Power Converter Offers Tunable Loop Feature



Gone are the days when power conversion devices forced system designers to reserve large amounts of board space for them. Along those lines, Lineage Power has introduced its MegaTLynx DC/DC 30, a power converter for distributed power architectures and intermediate bus voltage applications. The new power module is a high-efficiency, non-isolated, DC point-of-load (POL) converter. The MegaTLynx POL delivers exceptional thermal performance with full load capability at an ambient temperature of 85°C with only 200 linear feet per minute (LFM) airflow.

The Tunable Loop feature delivers leading density at the lowest cost implementation, leveraging standards-based Distributed-Power Open Standards Alliance (DOSA) footprints. Tunable Loop functionality allows design engineers to optimize the dynamic response of a DC POL power solution to match load requirements—reducing the quantity, type and size of the capacitors required for any given application. This DC power module operates over a wide range of input voltage from 6V to 14V and provides a precisely regulated output voltage from 0.8V to 2.75V, programmable via an external resistor. Available immediately worldwide, the Lineage Power MegaTLynx 30A POL is also available for multi-sourcing through licensees of the Tunable Loop technology. A ruggedized version for industrial and military applications will also be available.

Lineage Power, Plano, TX. (972) 244-9288. [www.lineagepower.com].

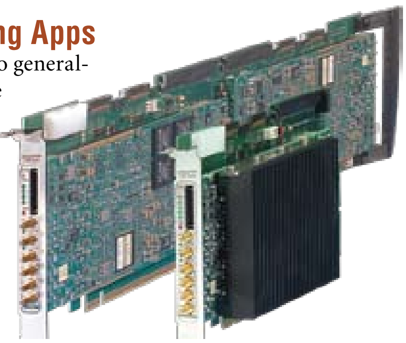
ARM Cortex-A5 Debuggers Supports Multiprocessing

The TRACE32 debuggers from Lauterbach now support the new ARM Cortex-A5 processor. The Cortex-A5 micro architecture is delivered within either a single core processor or a scalable multicore processor, the Cortex-A5 MPCore, which consists of up to four Cortex-A5 cores in a cluster. They are designed for applications that demand high performance and lower power consumption. The Cortex-A5 Embedded Trace Macrocell (ETM) provides non-intrusive program-flow trace capabilities for either of the Cortex-A5 processors for full visibility into the processor's instruction flow and enabling profiling analysis.

The TRACE32 tools further support the CoreSight technology for the Cortex-A5 processor. It extends the debug and trace capability to cover the entire system-on-chip including multiple ARM processors and DSPs. TRACE32 offers full OS-aware support for all popular operating systems running on asymmetric multiprocessing (AMP) or symmetric multiprocessing (SMP) systems.

Lauterbach, Höhenkirchen-Siegertsbrunn, Germany. +49 8102 9876-0 [www.lauterbach.com].

PCI Express Modules Target Beamforming Apps



High-performance data acquisition was once limited to general-purpose solutions. But as embedded board solutions have evolved, application-specific aspects and features have rolled into today's offerings. With that in mind, Pentek is introducing two beamformers to its expansive product line. Each is a high-speed software radio board for processing baseband RF or IF signals and incorporates unique and powerful beamforming functions. Created to accelerate system-level design and lower system cost, the boards bring high-performance built-in features and connectivity to PC platforms. The Pentek Models 7753 and 7853 differ in the number of channels and PCIe lanes; eight channels and x16 wide PCIe interface in the former, four channels and x8 wide PCIe interface in the latter. Each module houses up to four or eight 200 MHz, 16-bit A/Ds, each equipped with its own wideband digital down converter (DDC).

By daisy chaining two or more boards through a pair of high-speed connectors mounted on the edge of each module, the beamforming chain can extend beyond the four or eight channels on each board. Xilinx's Aurora protocol provides an efficient x4 point-to-point data path between boards at 1.25 Gbytes/s. Starting price for the 7753 and the 7853 begins at $15,795 and $14,195, respectively.

Pentek, Upper Saddle River, NJ. (201) 818-5900. [www.pentek.com].

Rugged 3U Carrier Card for XMC Is OpenVPX-Compliant

With last year's OpenVPX Working Group coming to fruition, compatible OpenVPX-based products are rolling out quickly. The latest from Curtiss-Wright Controls Embedded Computing is the 3U VPX VPX3-216 ExpressReach carrier card. It's designed to speed and ease the integration of XMC mezzanine cards (VITA 42.4) into embedded systems designed to be complaint with the OpenVPX (VITA 65) standard. The switchless VPX3-216 ExpressReach carrier card is the latest member of Curtiss-Wright Controls' expanding line of OpenVPX Ready 3U and 6U VPX cards designed to meet the new V1.0 OpenVPX and VITA 65 (Draft) Specifications.

The VPX3-216 ExpressReach provides a single XMC expansion site mapped directly to the backplane PCIe fabric, with no PCIe switches in between the card and the backplane that would require configuration and add latency. The card provides 64-bits of XMC I/O mapped as 20 differential pairs along with 38 single-ended signals mapped per VITA 46.9. It has been designed to operate with Curtiss-Wright or third-party XMC modules. This fully ruggedized carrier card expands the I/O capability of its host single board computer (SBC) without requiring the use of additional SBCs. The board is offered in a range of rugged configurations which include air-cooled (Level 0/100), conduction-cooled (Level 100/200) and VPX-REDI VITA48.1.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].

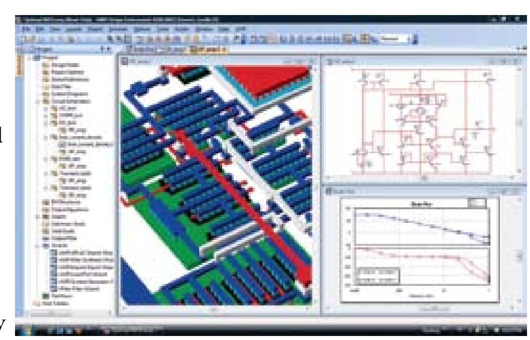
Scope Series Expands to Include 4 Channel and 40 MHz Models

Military systems continue to demand faster protocols and signaling bandwidths. That keeps the pressure on test equipment makers to keep pace. Along just such lines, LeCroy is expanding its WaveAce oscilloscope line to include 4 channel models from 60 MHz to 300 MHz and adding a new 2 channel, 40 MHz model. The 4 channel models provide 10 kpts/ch memory and up to 2 GS/s sample rate; the 40 MHz model provides 4 kpts/ch and a sample rate of up to 500 MS/s. All models offer long memory, color displays, extensive measurement capabilities and advanced triggering to improve troubleshooting and shorten debug time. With USB host and device ports, plus a LAN connection, the WaveAce oscilloscopes easily connect to a memory stick, PC or printer for saving data or remote control.

Available in bandwidths of 60 MHz, 100 MHz, 200 MHz and 300 MHz, the new 4 channel models provide a maximum sample rate of 2 GS/s and up to 10 kpts/ch memory or 20 kpts when interleaved. The long memory allows users to capture full sample rate acquisitions that are two to three times longer than the competition. The 40 MHz WaveAce 101 price is $695 while prices for the new 4 channel models range from $1,690 to $2,790.

LeCroy, Chestnut Ridge, NY. (800) 553-2769. [www.lecroy.com].

Analog Office Version 2009 Boasts High-Frequency IC Design Features



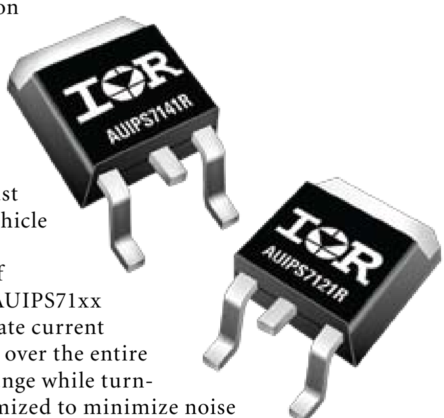
As high-speed communications and other hand-bandwidth signaling applications ramp up in the military, EDA software that's aimed at mixed-signal systems is become ever more important. Feeding that need, AWR has announced Version 2009 of its Analog Office high-frequency analog and RFIC design software. This latest release includes AWR's patent-pending multi-rate harmonic balance (MRHB) technology, which dramatically increases the speed and reduces the computer memory required to perform steady-state analysis of complex multi-tone designs such as those found in receivers and transmitters with multiple stages of upconversion and downconversion.

Analog Office Version 2009 also offers AWR's AXIEM 3D planar EM technology, which now supports 64-bit operating systems, multicore PCs and shape preprocessing algorithms that decrease solution time for complex geometries. Additional features in Analog Office Version 2009 include Automated Circuit Extraction (ACE), which provides improved extraction flow using frequency-domain interconnect modeling technology along with more traditional RLCK extraction. Also provided is Extract Flow. For very high-frequency designs, that allows the same layout to be effortlessly extracted to AXIEM software for full-wave 3D planar electromagnetic characterization. Version 2009 of Analog Office software is part of the AWR Design Environment (AWRDE), which is now shipping to supported customers.

AWR, El Segundo, CA. (310) 726-3000. [www.awrcorp.com].

Intelligent Power Switches for Harsh 24V Vehicle Systems

Engineers face a major hurdle designing vehicle junction boxes that meet tough new performance standards under short-circuit conditions. International Rectifier has introduced the AUIPS7121R and AUIPS7141R 65V high-side intelligent power switches (IPS) with accurate current-sensing and built-in protection circuits for harsh 24V vehicle environments. The new devices' over-current shutdown, over-temperature shutdown and active clamp circuit assure safe operation and protection under repetitive short circuit conditions. As a result of its protection features, the AUIPS71xx family can operate for extended periods of time, sustaining several millions of cycles under short-circuit conditions to provide a reliable robust solution for harsh 24V vehicle environments.

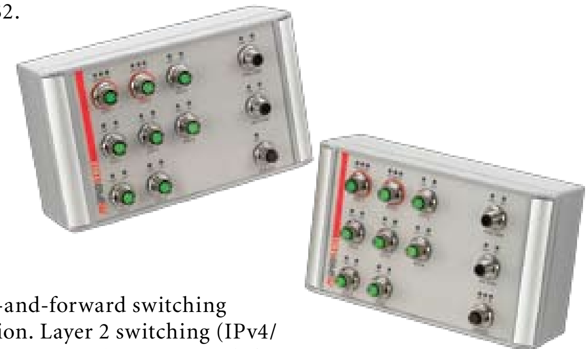


In addition to a host of protection features, the AUIPS71xx family provides an accurate current feedback of +/- 5 percent over the entire operating temperature range while turn-on and off-time are optimized to minimize noise in EMI-sensitive automotive applications. The devices are qualified according to AEC-Q100 standards; feature an environmentally friendly, lead-free and RoHS-compliant bill of materials; and are part of IR's automotive quality initiative targeting zero defects. Available in a DPAK package, pricing for the AUIPS7121R and AUIPS7141R begins at $1.40 each and $0.90 each respectively in 100,000-unit quantities.

International Rectifier, El Segundo, CA. (310) 726-8000. [www.irf.com].

Fanless, Ethernet Switches Offer Maintenance-Free Operation

Mission-critical defense applications can't tolerate their network links going down. Serving such needs, MEN Micro has expanded its new MIPIOS line of rugged embedded modular computers and components to include two new IP67-compliant Ethernet switches: the managed RS1 and the unmanaged RS2. Each features eight Fast Ethernet ports on standard M12 connectors with support for both full- and half-duplex operation as well as high-speed non-blocking and store-and-forward switching with auto-negotiation. Layer 2 switching (IPv4/IPv6), quality of service (QoS) support with four traffic classes IEEE 802.1p and three-level 802.1q security and an 8K MAC lookup table with automatic learning and aging are also standard on the switches. Two redundant power supplies provide a nominal 24 VDC, with a 9V to 36V input voltage range.

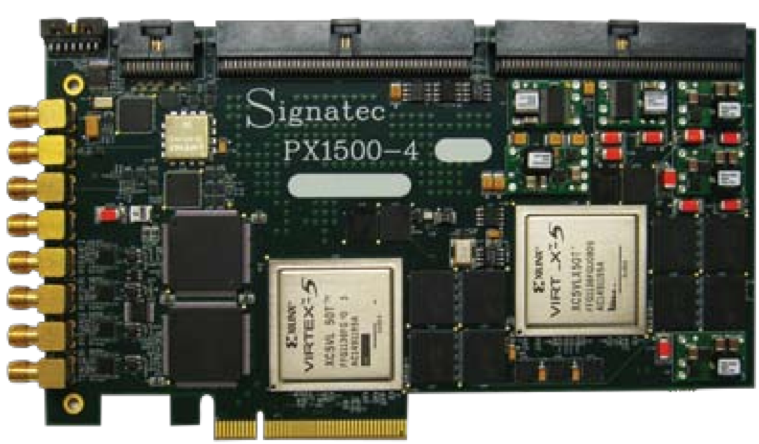


As part of MEN Micro's MIPIOS line, the new switches are fanless, maintenance-free and extremely rugged allowing them to perform reliably in the most demanding environments. The highly reliable, convection-cooled switches are fault-tolerant and automatically restore themselves, so if a link becomes unavailable temporarily, it will function correctly after the disturbance without the need for a reset or restart. The RS1 and RS2 also have a built-in test mechanism for increased reliability. Pricing for the RS1 is $1,733 and $1,153 for the RS2.

MEN Micro, Ambler, PA. (215) 542-9575. [www.menmicro.com].

PCI Express Digitizer Duo Comes in Four- and Two-Channel Flavors

Thanks to fabric interconnect technologies like PCI Express, military test systems can be integrated into compact desktop systems instead of racks of slot-card backplanes. Feeding such needs, Signatec announced the PX1500-4 high-speed digitizer, the most advanced PCIe-based wideband A/D board on the market. The PX1500-4 captures four synchronized channels at sampling rates up to 1.5 GHz, or two synchronized channels up to an amazing 3 GHz when interleaving the ADC data. 2 Gbytes of onboard memory configured as a large FIFO and a PCIe x8 bus ensures Signatec's PX1500-4 can continuously sustain long recordings at up to 1.4 Gbytes/s through the PCIe x8 bus (both mechanical and electrical) to PC disk storage without any break in the analog record.



Beyond its high-speed, multi-channel performance capabilities, the PX1500-4's frequency synthesized clock allows the ADC sampling rate to be set to virtually any value from 200 MHz, the minimum allowable ADC clock, up to 1500 MHz, offering maximum flexibility for sampling rate selection. Additional divide-by-two circuits are provided for sampling at even lower frequencies. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, 5 PPM reference clock or to an externally provided 10 MHz reference clock.

Signatec, Newport Beach, CA.

(949) 729-1084.

[www.signatec.com].

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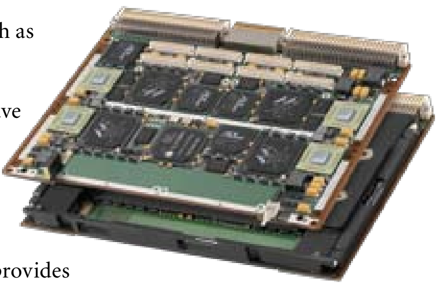
Clock Network Manager Supports LVDS and CMOS I/O

The importance of networking in today's military systems has brought with it a demand for reliable clock solutions. Aeroflex Colorado Springs has announced production of their UT7R2XLR816 Clock Network Manager, featuring eight independently programmable output banks. Bank programmability includes: frequency, I/O type (LVDS or CMOS), polarity, skew and voltage.

Aeroflex's UT7R2XLR816 is a flexible clock network management device, supplying up to 16 clock outputs over eight banks, with independent power supplies for each bank (+2.25V to +3.6V), giving the user greater flexibility in multi-voltage systems. Additionally, outputs can be configured as LVCMOS or standard LVDS pairs. An adjustable phase feature allows the control of phase on each output bank with respect to the reference clock. Applications such as high-altitude avionics, satellites, x-ray cargo scanners, test and measurement, networking, telecommunications and mass storage can take advantage of the UT7R2XLR816's low jitter (< 50 ps), wide operating range (24 MHz to 200 MHz) and a total dose tolerance of 100 krads(Si). The UT7R2XLR816 Clock Network Manager is available as QML Q and V for HiRel applications and has been assigned SMD # 5962-08243. Prototypes are available along with an evaluation board to support design development and debug. Production parts are priced at $1,825 for 100 quantity QML Q.

Aeroflex Colorado Springs, Colorado Springs , CO. (719) 594-8000. [www.aeroflex.com].

1.4 GHz Freescale 7448 VME Board Addresses Radar/Sonar Needs



Demanding applications such as radar, sonar, image processing and communications all have something in common: they have a seemingly endless appetite for DSP performance. With that in mind, GE Intelligent Platforms announced the G4ADSP rugged 6U VME multiprocessor. The G4ADSP provides improved processing performance with four Freescale MPC 7448 processors operating at up to 1.4 GHz; improved memory performance through the inclusion of up to 2 Gbytes of DDR memory; and improved I/O performance with the incorporation of four Gigabit Ethernet channels and PCI on P0. The G4ADSP is also a compelling upgrade path for existing users of the G4DSP since it provides form, fit and function compatibility with its predecessor, ensuring that customer migration is both straightforward and cost-effective.

The G4ADSP is also "AXIS-enabled," meaning that it supports GE Intelligent Platforms' AXIS Advanced Multiprocessor Integrated Software development environment. AXIS provides a quick start for application development and system evaluation with a suite of fully integrated modules for system development, visualization and deployment including example applications such as a distributed corner turn and stress tests.

GE Fanuc Intelligent Platforms, Charlottesville, VA. (800) 368-2738. [www.gefanuc.com].

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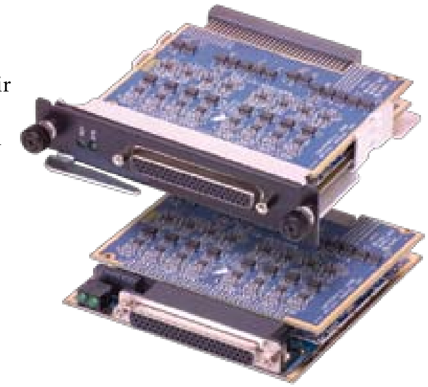
Synchro/Resolver Interface Cards Sport Dual ADC Channels



Avionics test systems are reaping the rewards of the multifunction board trend. Along just such lines, a pair of boards from United Electronic Industries is available in two models for a wide range of rotational position or motion applications. The DNx-AI-255 synchro/resolver interface boards are for use with UEI's PowerDNA Cubes and, in another form, for rack-mounting in a PowerDNR RACKtangle or HalfRACK chassis. Multiple operating modes ensure compatibility with all standard sensor wiring and excitation configurations. Each board has two fully isolated, synchro/resolver channels with independent A/D converters, and each channel offers 16-bit resolution, ±2.6 arc-minutes accuracy and scan rates up to 4000 Hz.

Each of the channels may be configured either as a synchro/resolver input with internal or external excitation or as a synchro/resolver simulated output. Each simulated output may be used as a software-controlled input stimulus for an avionics test system or flight simulator. Pricing for the DNA-AI-255 for Cube-based systems is $3,500 and for the DNR-AI-255 for RACKtangle or HalfRACK systems, $3,650.

United Electronic Industries, Walpole, MA. (508) 921-4557. [www.ueidaq.com].

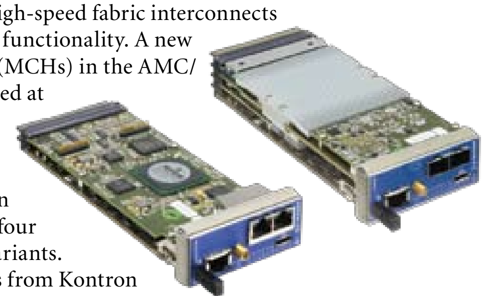
48-Channel Digital I/O PCIe Card Has Change of State Detection

No matter how much processing a military embedded system uses, ultimately it needs to connect to the real world—and that often means through digital I/O. A 48-channel PCI Express (PCIe) card has been designed for use in a variety of digital I/O applications. The PCIe-DIO-48S is compatible with 8255 PPI (mode 0), making it easy to program and migrate from other Acces I/O PCI digital I/O cards. The card features a x1 lane PCI Express connector that can be used in any x1 or higher PCI Express slot.

Each I/O line is buffered and capable of sourcing 32 mA or sinking 64 mA. Since the PCI Express x1 connector does not have sufficient power to drive this many channels, Acces provides an onboard Molex PC-style connector compatible with system power supplies (for disk drive power), to externally provide maximum 5V current sourcing capability. Connections to the card are made via two industry standard, 50-pin headers. Each header has three 8-bit I/O ports designated A, B and C. Each port can be programmed as inputs or outputs. Change of State (COS) detection and interrupt capabilities are designed to relieve software from polling routines that can consume valuable processing time.

ACCES I/O Products, San Diego, CA. (858) 550-9559. [www.accesio.com].

MicroTCA Carrier Hub Family Supports Four Fabric Types



MicroTCA is finding a niche in military applications—particularly those focused on marrying high-speed fabric interconnects with networking and comms functionality. A new line of modular carrier hubs (MCHs) in the AMC/MicroTCA form factor is aimed at fulfilling the management needs of data-intensive MicroTCA applications. With GbE, sRIO, PCIe or even 10 GbE fabrics, they support four different high-speed fabric variants. The AM4904/AM4910 MCHs from Kontron come in four versions: a pure Gigabit Ethernet switching MCH, in combination with a PCIe mezzanine or with sRIO, and for high-bandwidth demands, with 10 Gigabit Ethernet switching.

Equipped with a 600 MHz PowerPC 405EX processor for MCMC functionality and switching management, they enable highly efficient, redundant system architectures with up to 12 AMCs, two cooling units and four power units. All Kontron AM4904/AM4910 MCHs feature a clock implementation and a PCI Express fabric clocking distribution. They also include high-performance features such as a wire speed, Enterprise-Class Ethernet switch with Layer 2 switching and Multi-Cast support including full 4K VLANs and link aggregation, quality-of-service support (QoS) and a packet classification engine for flexible access control lists.

Kontron, Poway, CA. (888)-294-4558. [www.kontron.com].

1U Rackmount Appliance Serve Core2 Quad Processor

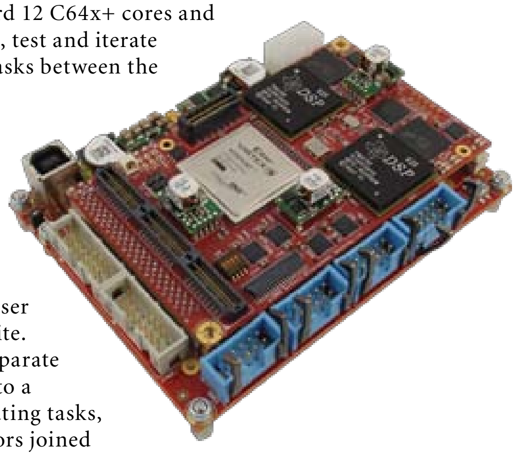
The 1U server form factor has secured a key niche among military system designers. It provides a compact computing solution that's compatible with a variety of off-the-shelf networking gear like routers. A high-performance 1U rackmount appliance supports a broad range of network services for the enterprise and small businesses. The PL-80140 from Win Enterprises supports the Intel Core2 Quad processor and provides processing scalability with support for Pentium Dual Core and Celeron D.

The Intel Core2 Quad Processor is designed to handle intense compute and visualization workloads for highly threaded applications. The PL-80140 couples the Intel Core2 Quad processor and a 1333 MHz Front Side Bus. The unit is designed with Intel Embedded IA components warranted for longevity to provide long product life. A high-bandwidth dual-channel DDRII DIMM socket supports 800/667 memory with up to 4 Gbytes at 800 MHz. The unit is available with six Gbit Ethernet ports through PCI-E x1 interface and offers four ports of optional bypass function. The PL-80140 delivers high throughput for a broad range of network applications. Pricing begins at $554 in OEM quantities.

WIN Enterprises, North Andover, MA. (978) 688-2000. [www.win-ent.com].

Development Platform Features Latest TI Multicore DSP

While military system designers have been expanding their demands for digital signal processing, one thing hasn't changed: Developing DSP-based systems is a level of complexity above the standard general-purpose processor systems. Easing the way, the EVP6472 from Sundance Multiprocessor Technology is a multiprocessor, multicore development solution for Texas Instruments (TI) TMS320C6472 Digital Signal Processors (DSPs). It features design support from the Diamond multiprocessor tool-suite from 3L. Diamond enables easy access to the onboard 12 C64x+ cores and allows the designer to rapidly build, model, test and iterate different design architectures by moving tasks between the processor cores.



The EVP6472 is provided with a TIM carrier card and a modular plug-in that features dual C6472 multicore DSP, a Virtex5 FX30 FPGA with embedded PowerPC, two banks of DDR2 memory, Rocket Serial Link (RSL) connectors and a host USB 2.0 interface. The development platform is supported by TI's Code Composer Studio (CCS) and the 3L Diamond tool-suite. The Diamond suite allows developers to separate the implementation of their application into a software section based around communicating tasks, and a hardware section built from processors joined by data-transfer links. For a time-limited period, pricing starts at $2,000.

Sundance Multiprocessor Technology, Chesham, UK. +44 1494793167. [www.sundance.com].

Development System Marries Blackfin and .NET Micro Framework

The FPGA Mezzanine Card (FMC) form factor, also called VITA 57, takes advantage of the trend toward complete subsystem functionality now possible on today's FPGAs. The Analog Devices BF518F FMC Development Kit from Avnet Electronics Marketing offers hardware and software design engineers the flexibility they need by providing an I/O mezzanine card, electrically compatible with the FMC VITA57 specification. This feature enables the connection to FMC carrier cards and facilitates the development of applications using the Analog Devices BF518F Blackfin processor with FPGAs.

By enabling the .NET Micro Framework on this board, the developers now have access to programming models and tools, including Visual Studio, that have made the desktop environment productive while maintaining the access to the underlying hardware that is needed. The virtualization of the hardware "future proofs" the applications so that work done on these development platforms can migrate easily to the eventual products. The kit is available for $349, or $499 with the add-on debug agent board.

Avnet Electronics Marketing, Phoenix. AZ. (800) 408-8353. [www.avnet.com].

3U OpenVPX Systems Available as Air- and Conduction-Cooled

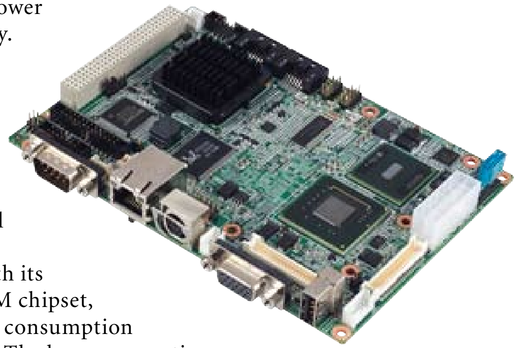
Two OpenVPX-compliant 3U development systems cover both air- and conduction-cooled projects. Just announced by Extreme Engineering, the XPand1200 is a development platform for conduction-cooled modules, and the XPand1300 is designed for air-cooled modules. Both support a minimum of ten 0.8-inch or 1.0-inch pitch slots and are built in accordance with OpenVPX design principles. The XPand1200 conduction-cooled development system features rapid I/O configuration via rear transition modules (RTMs), star PCIe and Gigabit Ethernet topologies, including PCIe and Gigabit Ethernet switch. The XPand1200 supports up to 550W of total simultaneous power delivery and a thermal dissipation of up to 50W per slot. The unit weighs 38 pounds—including backplane and power supply—and measures 8.5 x 11 x 13 inches.

The XPand1300 air-cooled development system also features rapid I/O configuration via RTM modules, removable side covers for debug access, star PCIe and Gigabit Ethernet topologies, including PCIe and Gigabit Ethernet switch. Up to 20 CFM of airflow is provided per slot as well as 550W of total simultaneous power delivery. The XPand1300 provides the system developer maximum performance and flexibility, weighing only 19 lbs, including backplane and power supply, and measuring 13.5 x 13.5 x 11.6 inches. The XPand1200-1 and XPand1300-1 system configurations are available now for $7,500, including backplane, switch and RTM.

Extreme Engineering Solutions, Middleton, WI. (608) 833-1155. [www.xes-inc.com].

Atom-Based 3.5-inch SBC Provides Dual LVDS

The Atom processor has caught on like wildfire in military applications—especially where Size, Weight and Power (SWaP) is a priority. Advantech has released a new 3.5-inch SBC called the PCM-9361. The PCM-9361 is driven by the small and powerful 45nm Intel Atom N270 processor with its 945GSE and ICH7M chipset, offering low power consumption in a fanless design. The low power rating of the Atom architecture consumes only 10W of power and provides rich I/O functionality. The PCM-9361 supports multiple display outputs including: 36-bit LVDS1, 48-bit LVDS2, CRT and 18-bit TTL LCD.

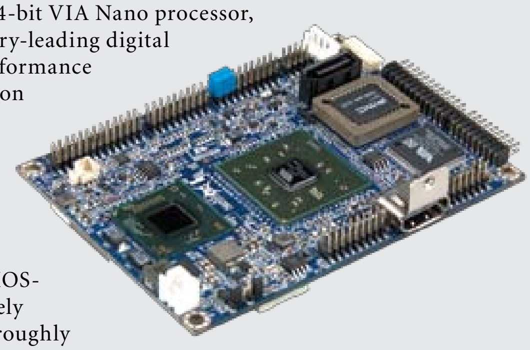


The PCM-9361 is a 3.5-inch form factor (146 x 102 mm) SBC, one of the most popular embedded form factors with the same size as a 3.5-inch floppy drive. The PCM-9361 was designed with compact low-profile considerations; its total height, including the fanless heatsink, is only 27 mm—making it suitable for a 1U chassis design. The PCM-9361 is very versatile and can support all kinds of 32- and 48-bit display configurations ranging from 800 x 600 to 1920 x 1080 resolutions. The PCM-9361 with its Intel 945GSE chipset uses the integrated Intel GMA950 graphic engine and supports Microsoft DirectX 9.1 and multiple displays.

Advantech, Irvine, CA. (800) 866-6008. [www.advantech.com].

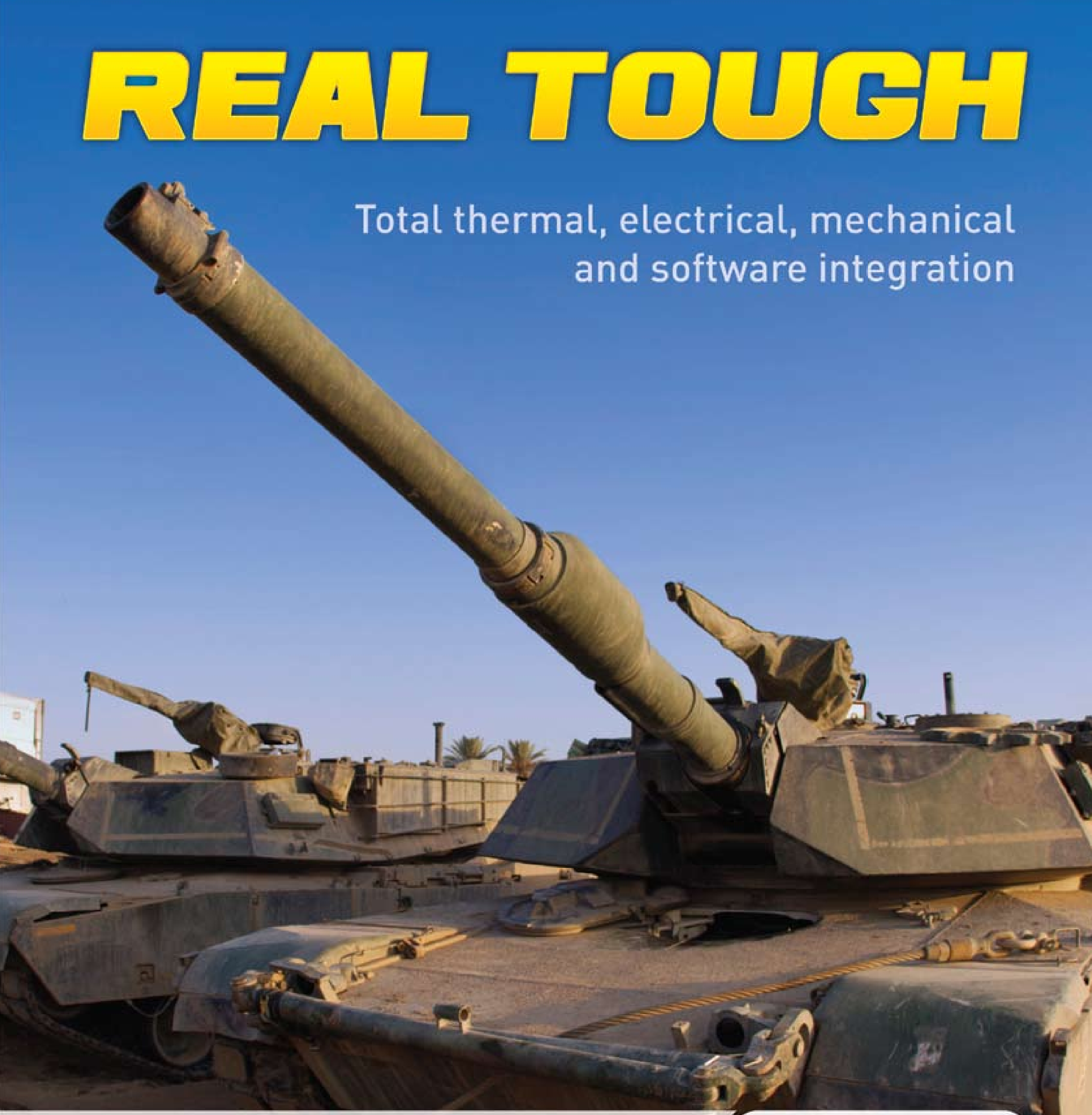
Fanless Pico-ITX Board Sports VIA Nano Processor

Compact, low-power, fanless SBCs are just what the doctor ordered in deployed military systems. VIA Technologies offers the VIA EPIA-P820, the first Pico-ITX form factor board to feature the high-performance, 64-bit VIA Nano processor, bringing industry-leading digital multimedia performance and virtualization capabilities to the smallest of spaces with the VIA AMOS-3001 chassis system.



The VIA AMOS-3001 is an entirely fanless and thoroughly robust chassis system that is specially designed to work with the VIA EPIA-P820. Leveraging the digital prowess of the VIA EPIA-P820, the VIA AMOS-3001 offers a powerful, rugged and HD-ready industrial-class PC that combines all the benefits of high performance 64-bit computing and ruthless hardware acceleration of HD media across the latest display connectivity standards including native HDMI support. The ultra-compact VIA EPIA-P820 supports 2 Gbytes of DDR2 system memory and leverages a power-efficient, high-performance 1.2 GHz U2500 VIA Nano processor that measures a mere 10 cm x 7.2 cm. The VIA EPIA-P820 uses a specially designed I/O add-on board, which supplements the native HDMI port to add a VGA port, a Gigabit LAN port and two USB 2.0 ports.

VIA Technologies, Fremont, CA.
(510) 683-3300. [www.via.com.tw].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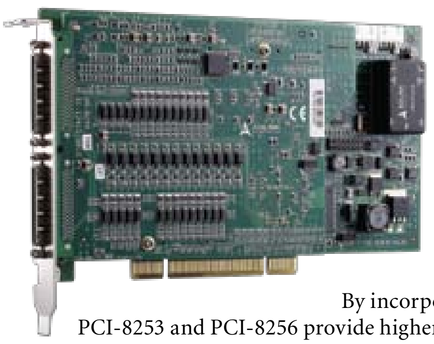
DSP-Based Motion Controllers Offer Full Closed-Loop Control

Two DSP-based servo motion controllers handle three or six axes of control. The PCI-8253 (three axes) and PCI-8256 (six axes) from Adlink are designed to take full advantage of the latest digital signal processing technologies to provide a ±10V analog motion controller with full closed-loop control, a PID plus feed-forward algorithm and 20 MHz encoder input frequency. By incorporating a DSP, the PCI-8253 and 8256 are able to provide advanced, flexible and comprehensive motion functions that cannot be achieved through ASIC-based solutions.

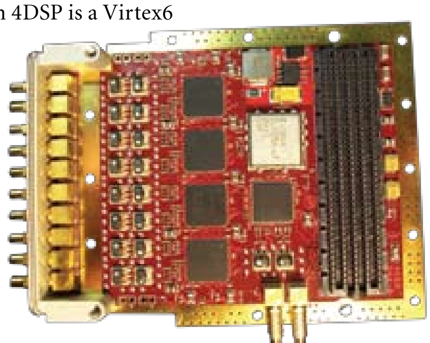


By incorporating FPGA technology, the PCI-8253 and PCI-8256 provide higher motion control performance by a fast encoder input frequency up to 20 MHz. In addition, the hardware-based high-speed position comparison and trigger output speed of up to 1 MHz further make the PCI-8253/8256 ideal for AOI applications. The PCI-8253 and PCI-8256 also offer a point table that supports over 5,000 points for each axis, ideal for contouring applications. The PCI-8253 and PCI-8256 are currently available for a list price of $1,329 and $2,129, respectively.

ADLINK, San Jose, CA. (408) 360-0200. [www.adlinktech.com].

Multi-Camera Image Processor Card 350 Mpixels/s Streams

Designed to serve real-time multi-camera image processing applications such as used by the military in situational awareness applications, the VID675 from 4DSP is a Virtex6 FPGA-based XMC real-time multi-camera image processor board. The VID675 is designed for processing of high frame-rate, high pixel-density digital video streams from multiple camera. The VID675 offers abundant FPGA logic resources for specialized image processing prior to image compression, a power house for real-time pre- and post-compression image processing. The VID675 features six codec JPEG2000 or H264/MPEG-4 hardware compression devices (CODECs) based on the Analog Devices ADV212, capable of up to 350 Megapixels/s sustained performance allowing simultaneous compression of 16 colored video streams 640 x 480.



The VID offer several camera interface options, Full Camera-Link, Dual Base Camera-Link, 16 Channel NTSC, 36-pair LVDS and quick-spin customer-specific interface options, available on a request-for-quotation (RFQ) basis. The VID675 image processor is complemented by 4DSP's engineering services program, where specific FPGA algorithmic processes are developed to meet customer's unique and specifically defined requirements.

4DSP, Reno, NV. (800)-816-1751. [www.4dsp.com].

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Coming Next Month

COTS JOURNAL

Special Feature: ISR Programs and Payloads in Large UAVs The DoD has adopted a strategy of closely pairing its intelligence, surveillance and reconnaissance (ISR) programs with its UAV programs. This section explores how "mission autonomy" is becoming a goal today's large UAV system designs. Next-generation UAVs are replacing the multiprocessing of big, power-hungry boards based on general-purpose processors like the PowerPC-based boards, with more integrated boards sporting FPGAs. This section looks at how this system consolidation is impacting the radar, imaging processing and communications capabilities of next-gen large UAVs.

Tech Recon: Power Supplies Attack the SWaP Challenge Reducing Size, Weight and Power (SWaP) is among the most critical design priorities in a variety of today's military systems. Power supplies and power conversion electronics rank as a make or break technical choice in achieving those goals. With more and more computing stuffed into smaller spaces, power has direct implications on the size, cooling and mobility of a system. Articles in this section examine technology trends affecting DC/DC converters, power supply module bricks and slot-card power supplies (VME, cPCI and others).

System Development: Vehicle-based Networking and SatCom When the Army issued the directive to armor all tactical vehicles to protect our soldiers from weapons such as Rocket Propelled Grenades (RPGs) and Improvised Explosive Devices (IEDs), the pressure was on to reduce the weight budget left over for the electronics aboard vehicles. For SATCOM On-the-Move systems, that means systems integrated into a much smaller volume, compared to the current-generation systems. System designers are consolidating their architectures relying heavily on server computer blades and subsystems in 1U form factors and/or CompactPCI. This section examines the efforts underway to accomplish mobile satellite comms in half the space, and considerably less weight.

Tech Focus: Conduction-Cooled Compact PCI The CompactPCI embedded form factor has achieved the maturity and broad product range that military system designers so crave. Now well into its second decade of existence, the 3U flavor of cPCI is particularly attractive to space/weight-constrained applications like avionics. This Tech Focus section updates readers on cPCI trends, and provides a product album of representative conduction-cooled 6U and 3U cPCI boards.

COTS

Editorial

Jeff Child, Editor-in-Chief

Onward and Up the Complexity Curve

Here we are at 2010. Here's wishing you a happy and prosperous year ahead. While we may not have flying cars and manned spaceships exploring Saturn's moons quite yet, 2010 certainly feels like the future. Military electronic systems—across all branches, manned and unmanned, large and small—continue to head in the direction of increasing complexity as programs require ever more functionality, autonomy and intelligence.

That's all good for our segment of the industry because, naturally, that drives demand for faster embedded computing and other more sophisticated electronic subsystems of every kind. That upward trend in complexity, while perfectly in line with the idea of always improving the warfighter's ability to do their jobs better, does come at a price. It's no big secret that the defense industry has felt the downsides of growing complexity in a more profound way than other industries. Costs of major programs inevitably grow significantly over budget while average program development cycles have grown by up to 20 percent over the last decade—and predicting accurate development cycles seems to be getting harder.

All kinds of attempts have been made to mitigate those overruns through the "top down" acquisition. Some progress in terms of understanding the weaknesses in structure, process and governance of acquisitions has been made, but significant cost/schedule overruns still persist. The latest efforts at tackling these issues come from the Defense Advanced Research Projects Agency (DARPA), taking what could be called a "bottom up" strategy of reforming the engineering process side of things.

DARPA sometimes chooses its research by doing what it calls a Broad Agency Announcement (BAA) process. Last fall DARPA released a BAA soliciting research proposals for a program called META. The goal of META is to "substantially improve the design, integration/manufacturing and verification of complex cyber-physical systems, and particularly aerospace and defense systems such as aircraft, rotorcraft and ground vehicles." The term "cyber-physical systems," as you might guess, is cringe-worthy jargon for people like me in the wordsmithing business. DARPA defines cyber-physical as systems that derive significant portions of their functionality from both software and electromechanical systems. Virtually all defense platforms—aircraft, spacecraft, naval vessels, ground vehicles—and systems-of-systems fall under that rubric, as do automobiles, power grids, air traffic control systems and integrated circuits. I prefer to cut to the chase and use the term "embedded system" instead, but that's just me.

Last month DARPA held an Industry Day event to review proposals from the various companies interested in pursuing the program. Looking at some of the material from the introductory part of the event, I saw a chart from Paul Eremenk's presentation that blew me away. Eremenk is with DARPA's Tactical Technology Office. It should be a fascinating comparison between the mil/aero industry, the automotive industry and the integrated circuit industry. The chart graphed complexity—measured in parts count plus lines of software source code—versus design, integration and testing time (in months). The IC industry, as the chart showed, stayed at a relatively fixed development cycle time as complexity increased. The automotive industry meanwhile has moved steadily down in development time as cars have grown in complexity. Meanwhile aerospace and defense systems have, over the same timeframe, ramped ever upward in development time and associated cost as complexity increased. To me, the chart is a very vivid illustration of what happens when some industries revamp their design flows, and others don't.

As the chart showed, the idea behind the META program is that, while the complexity of aerospace and defense systems has grown considerably over the past half-century, the systems engineering approach—or, more specifically, the design, integration/ manufacturing and test flow—really hasn't changed since back in the days of Atlas missile development and Apollo programs—which were codified in MIL-STD-499.3.

DARPA called for proposed research under the META program to investigate innovative approaches that enable revolutionary advances in this area. Specifically excluded is research that primarily results in evolutionary improvements to the existing state of practice. The ultimate goal of the META program is to make a dramatic improvement on the existing systems engineering, integration and testing process for defense systems. According to DARPA, META isn't intended to revolve around any one particular alternative approach, metric, technique, or tool. Rather it aims to develop model-based design methods for embedded systems—or cyber-physical systems as they call it—that are far more complex and heterogeneous than those common today.

As someone who has closely followed all the major vendors of system modeling tools and frameworks over the years, I'm having a hard time understanding what exactly the META program will result in that's fundamentally different than what's already available in today's very sophisticated embedded system development tools market. That said, there's never been any such effort—to my knowledge—that's been built from the ground up specifically for the defense and aerospace industry. One challenge is the priority that military systems have on rugged environment features and strict goals for size/ weight/power minimization at the subsystem and component level. It's all very interesting at any rate, so I'll be keeping an eye on META as it moves forward.

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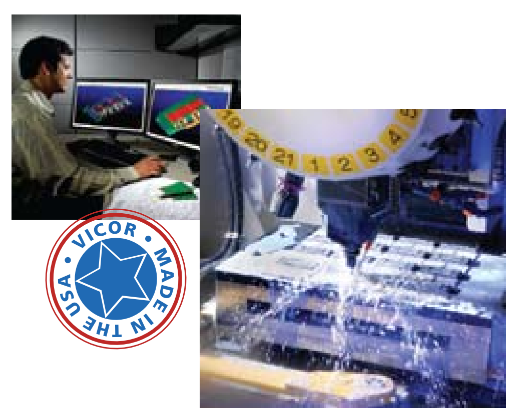

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